A Fault Detection and Protection Scheme for Three-Level DC–DC Converters Based on Monitoring Flying Capacitor Voltage

Honggang Sheng, Fei (Fred) Wang, *Fellow, IEEE*, and C. Wesley Tipton IV

***Abstract*—Fault detection and protection is an important design aspect for any power converter, especially in high-power high-voltage applications, where cost of failure can be high. The three-level dc-dc converter and its varied derivatives are attractive topologies in high-voltage high-power converter applications. The protection method can not only prevent the system failure against unbalanced voltage stresses on the switches, but also provide a remedy for the system as faults occur and save the remaining components. The three-level converter is subject to voltage unbalance in certain abnormal conditions, which can result in switch overvoltage and system failure. The reasons for the unbalanced voltage stresses are fully investigated and categorized. The solutions to each abnormal condition are introduced. In addition to the voltage unbalance, the three-level converters can be protected against multiple faults by the proposed protection method through monitoring the flying capacitor voltage. Phenomena associated with each fault are thoroughly analyzed and summarized. The protection circuit is simple and can be easily implemented, while it can effectively protect the three-level converters and its derivatives, which has been verified by the experiment with a three-level parallel resonant converter.**

***Index Terms*—Flying capacitor, protection, three-level dc-dc converter, voltage unbalance.**

I. Introduction

RELIABILITY is always a concern for power converters. Faults can occur even in carefully designed circuits. Fault detection and protection is an important design aspect for power converters, especially in high-power high-voltage applications, where cost of failure can be high and the consequence of failure can be serious. For dc–dc high-voltage high-power converter applications, the three-level dc–dc converter and its varied derivatives are attractive topology choices [1]–[13]. Fig. 1 shows a three-level parallel resonant dc–dc converter as an example. The main advantage of three-level dc–dc converters is that the main switches only withstand half of the input dc-link voltage, so lower voltage rating devices with better performance can be used. On the other hand, three-level converters need to have balanced dc voltages Vcin1 and Vcin2 and two clamping diodes to ensure proper operation and equal voltage sharing [14]. The flying capacitor is initially introduced by Fransisco for the phase shift operation [15]. The flying capacitor can help to decouple the switching transition of the outer two switches (S1 and S4) and the inner two switches (S2 and S3). When one of the outer switches turns OFF, its parallel capacitor is charged, and meanwhile the parallel capacitor of the other outer switch is discharged through the flying capacitor so that zero voltage switching (ZVS) can be achieved. The two capacitors in parallel with the inner two switches do not participate in this switching transition and vice versa. Furthermore, with phase shift pulse width modulation (PWM) control, the flying capacitor is essentially connected in parallel to the input capacitors during the freewheeling stage of the converter alternatively. Therefore, the flying capacitor can alleviate the voltage imbalance of the input capacitors with phase shift PWM operation [16]. In addition, the flying capacitor also works as a snubber capacitor for the two inner switches. Under normal operating conditions, Vcss should have a nominal voltage equal to Vin/2. An abnormal Vcss may indicate an abnormal circuit condition or fault, which can be used as the basis for fault detections.

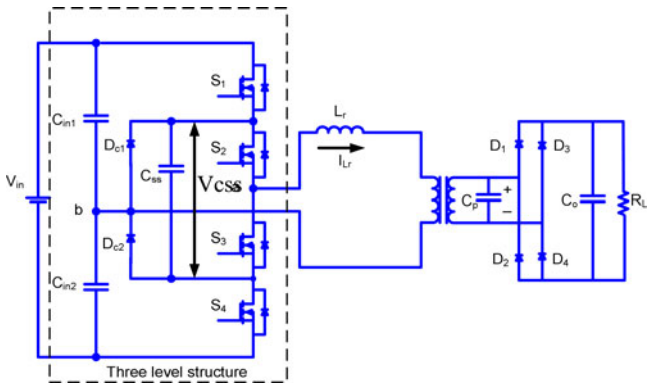

Fig. 1. Topology of a three-level parallel resonant converter.

There have been previous studies on the protection of three-level inverters or other types of dc–dc converters [17]–[26]. However no study has been conducted specifically for the protection of three-level dc–dc converters. An inverter protection

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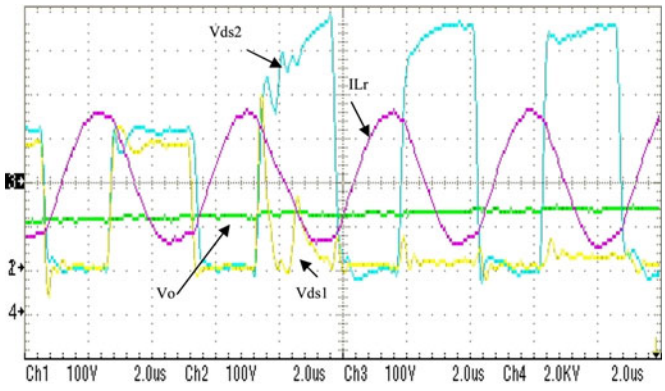

Fig. 2. S1 failure of short-circuit without the protection circuit. [Vds1 (100 V/div),Vds2 (100 V/div), Iin (100 A/div), Vout (2 kV/div), 2 us/div]

against unbalanced voltage of the dc-link capacitors based on a neutral point voltage detection has been proposed in [26]. Although this method can be applied to a three-level dc–dc converter, only limited problems can be detected by the neutral point protection. One real failure was captured in our laboratory, shown in Fig. 2. The switch S1 suddenly has a short-circuit failure so that the other device S2 in the same leg with S1 has to withstand the full input voltage while the neutral point voltage is still normal. Since no protection circuit can detect this fault, S2 finally failed after around 300 us, as well as the other two switches in the other leg. Furthermore, the neutral point detection is less sensitive due to the relatively large input capacitance compared with the flying capacitor.

The proposed protection method is based on the detection of Vcss. As will be explained in later sections, the advantages of this protection scheme include the following.

1) No additional components on the power stage are added, not even additional current sensors; therefore there is no impact on normal converter operation and performance.
2) Sensitivity to unbalanced switch voltages and the ability to detect multiple faults.
3) Fast response time that is very critical in short-circuit and shoot-through protection.
4) Low cost and easy implementation.
5) Can replace under/over input voltage lockout.

The rest of this paper is organized as follows. First, with the traditional operation schemes, the reasons that cause the abnormal voltage stresses are thoroughly analyzed and categorized, as well as the solutions according to the different reasons. In essence, these issues can be fixed or avoided in a normal converter design and operation, as is stopped by protection circuit. Then the possible faults of the three-level parallel resonant converter (PRC) are systemically analyzed and summarized with the help of simulation in Section III. In Section IV, a protection circuit with fast response time is presented, along with the flying capacitor design and the circuit design criteria. Finally, Section V provides experimental results to verify the analysis and the protection functions.

II. Operation Principle and Solutions to Unbalanced Voltage Stresses

The typical waveforms for three-level parallel resonant converter with phase-shift (PS) and PWM operation modes are illustrated in Fig. 3(a) and (b). Since both operation modes have to guarantee that the outer switch (S1 or S4) should be turned OFF no later than the inner switch (S2 or S3) in the same leg for ZVS achievement, the analysis in the paper will be the same for both operation modes.

Reference [27] has analyzed the problem of voltage unbalance across the switches in the same leg at two specific conditions, with open voltage loop control and at light load. However, Vcss could also be changed under other various conditions, such as zero-current-switching (ZCS)/non-zero-voltage-switching (ZVS) operation, high voltage ripple on input capacitors, unbalanced switching timing, etc. In essence, these can be fixed when the problem is stopped by protection and located. The solutions to the issues are introduced. A thorough analysis on abnormal conditions is necessary for designers to understand the converter operation and know the limits so that a protection can be designed to tolerate to normal operation without losing sensitivity.

These abnormal conditions can be classified into three main categories, as enumerated in the following.

A. Abnormal Input Capacitor Voltages Due to Input Voltage

As shown in Fig. 1, two input capacitors (Cin1 and Cin2) are needed to split the input voltage equivalently, and the neutral point, Point b in Fig. 1, has half of the input voltage ($V_{\rm in}/2$). So the neutral point voltage and Vcss are fundamentally determined by the input voltage. If the input voltage varies beyond the allowed range, obviously, the over/under input voltage lockout can be triggered by monitoring the Vcss.

B. Abnormal Input Capacitor Voltages Due to Unbalanced Neutral Point Voltage

Another main abnormal performance of input capacitor voltages is unbalanced voltage. When the voltage across Cin1 is higher than $V_{\rm in}/2$, the flying capacitor will be charged through down clamping diode Dc2, shown in Fig. 4. If the Cin2 voltage is higher than $V_{\rm in}/2$, the flying capacitor will be charged through clamping diode Dc1, shown in Fig. 5. More explicitly, the flying capacitor will be paralleled with the input capacitor which has high voltage stress. It should be noted that this is also why the flying capacitor helps to alleviate the voltage unbalance of the input capacitors mentioned in [16]. No matter which input capacitor has higher voltage, or, in other words, no matter the neutral point has higher or lower voltage than $V_{\rm in}/2$, the flying capacitor voltage will be charged to the peak voltage of the input capacitor with a higher voltage. So unequal capacitances of input capacitors, unbalanced duty cycles or mismatched switching timings, etc., belong to this case, which contributes the unbalanced input capacitor voltages and then the abnormal flying capacitor voltage. When the problem is caused by these issues, it can be easily solved in circuit. Normally these tiny unbalanced

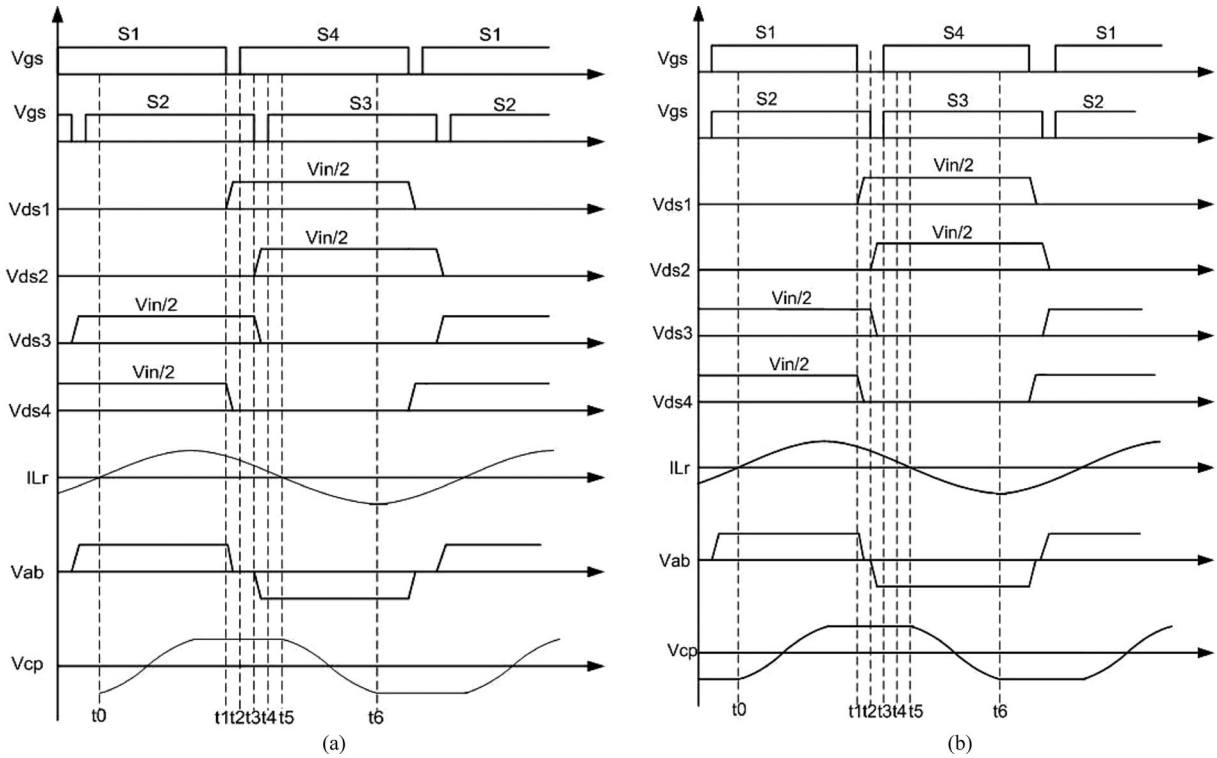

Fig. 3. Principal waveforms. (a) PS operation mode. (b) PWM operation mode.

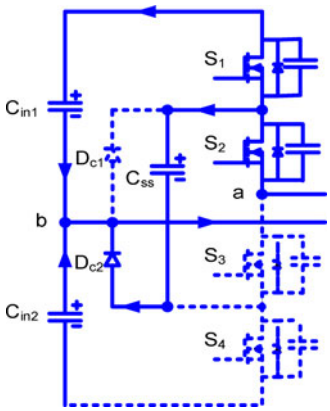

Fig. 4. Charging loop when the voltage of Cin1 is higher than half of the input voltage.

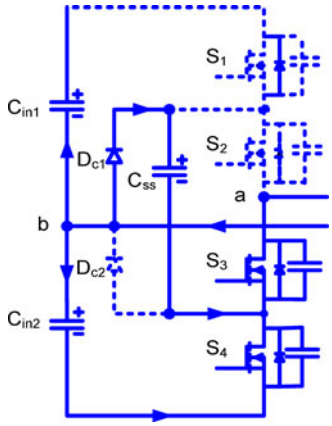

Fig. 5. Charging loop when the voltage of Cin2 is higher than half of the input voltage.

capacitances and duty cycles can be tolerated without serious consequence. In addition, the unbalanced duty cycles can be alleviated by the flying capacitor in the phase-shift operation. A control circuit to balance the unsymmetrical duty cycles by monitoring voltage across the flying capacitor for the nonphase leg structure converter, such as buck, boost has been proposed in [28]. It also can be adjusted for the circuit with the phase leg structure when the unbalanced duty cycle is an issue.

Moreover, even if the voltages across the input capacitors are balanced, the Vcss still can be influenced by the voltage ripple on the input capacitor. According to the earlier analysis, the peak voltage on the input capacitor will pump energy to the flying capacitor and thus Vcss can be calculated with the following:

$$V_{\rm css} = \frac{(1+k)}{2} V_{\rm in} \tag{1}$$

where $V_{\rm in}$ is the input voltage, and k is the allowed voltage ripple percentage for input capacitors, which usually is determined by (2). This can explain why the Vcss increases slightly even in a normal operation

$$k = \frac{2 \cdot I_o}{C_{\rm in} \cdot f_s \cdot V_{\rm in} \cdot V_{\rm in} \cdot \eta} \cdot 100\% \tag{2}$$

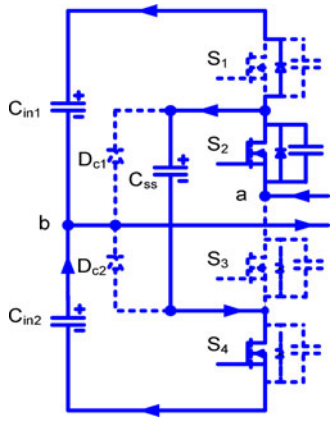

Fig. 6. Charging loop for wrong operation mode of ZCS instead of ZVS.

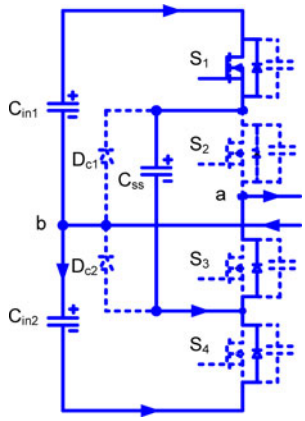

Fig. 7. Charging loop due to reverse switching timing.

where I_o is the output current, $C_{\rm in}$ is the capacitance for one of the input capacitors, f_s is the switching frequency, $V_{\rm in}$ is the input voltage and $\eta$is the converter efficiency.

C. Losing Discharging Path Even With Normal Input Capacitor Voltages

Even if the neutral point voltage is normal, the unbalanced voltage stresses still can happen in some conditions. In a normal operation, the flying capacitor can be charged through the upper clamping diode (Dc1) or S1. Or it can be charged through bottom clamping diode (Dc2) and S4 due to the symmetrical structure. The only possible discharging path for flying capacitor is through S2 or S3. If the flying capacitor can be charged through S2 or S3 instead of discharging in some conditions, the flying capacitor voltage will definitely increase because it has no way to decrease.

With the conventional ZVS control (S1 is turned OFF before S2, and S4 is turned OFF before S3), the commutation of the phase shift provides a discharge loop for flying capacitor when ZVS operation is desired. However, when the converter loses ZVS, such as at light load; or the switching timing is wrong, such as when S2 is switched OFF before S1 or S3 is switched OFF before S4; the flying capacitor will be charged instead of being discharged. The Vcss could increase to approximate the input voltage due to no discharging loop. Fig. 6 shows an abnormal case of the accidental ZCS operation mode. The current in the inductor has changed its direction when S1 is turned OFF. The upper side of the flying capacitor is connected with the input voltage through the body diode of S1. And the bottom side of the flying capacitor is connected with the ground when S4 is turned ON after S1 is OFF. In this case, the flying capacitor will be charged to full input voltage instead of discharging. Due to the symmetrical structure, this case can happen when S1 is turned ON after S3 is OFF. At light load, if the converter loses the ZVS operation for the lagging switch, or even worse, loses ZVS for both leading switch and lagging switch, the mechanism is the same as the ZCS condition. In order to solve this issue, ZVS has to be guaranteed in the three-level converter design for all of its operation conditions, from heavy load to light load.

Fig. 7 shows another case of reverse switching timing. When S2 is turned OFF before S1, the upper side of the flying capacitor is connected to the input voltage through S1 and the lower side of the flying capacitor is connected to the ground through the body diode of S4. Thus, the flying capacitor suffers the full input voltage. In order to solve this problem, the switch sequence has to be assured. Minimal phase-shift is desired to reduce the duty cycle loss when the regulation is through varying frequency instead of the duty cycle. If the abnormally high Vcss is owing to slightly too small phase shift, enlarging the phase shift or paralleling external capacitors in the inner switches is an effective way to solve this problem. However, it should be noted that the increased capacitance on the inner switch will worsen its ZVS condition.

III. Multiple Faults in the Three-Level Converter

This section analyzes the behavior of the flying capacitor voltage Vcss under various fault conditions in the three-level parallel resonant converter shown in Fig. 1. Fig. 8 illustrates the most common faults associated with the active devices and load, including open- or short circuit of main switches S1 and S2, clamping diodes Dc1, antiparallel diodes D1 and D2, rectifier diode Dr1 and load. The antiparallel diodes D1 and D2 short circuit will be the same as the corresponding main switch short circuit, only the open circuit of these antiparallel diodes need to be included. When the main switch is MOSFET, its body diode is commonly used as antiparallel diode instead of the external diode. It should be noted that the main switch cannot work properly if its body diode fails. Due to the symmetrical structure, the results will be the same as the counterpart failures occur. To some extent, the fault condition is the worst case of these abnormal conditions. For example, when S2 fails to open circuit, it is like avoiding the rule that S2 should be turned OFF no earlier than S1.

A. Outer Switch Open Circuit

If outer switch (e.g., S1) has an open circuit, the loop is still complete for inductive load current so that the energy in

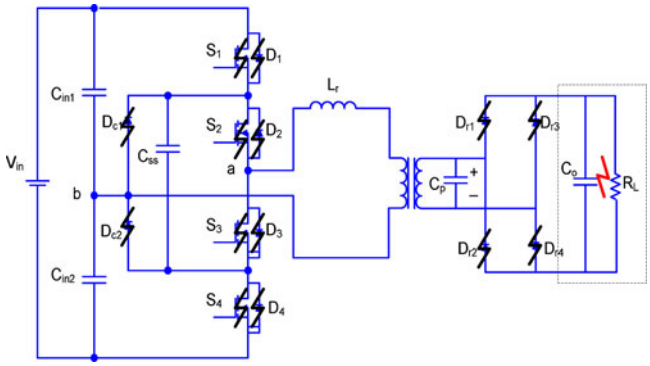

Fig. 8. Possible faults on the three-level parallel resonant converter.

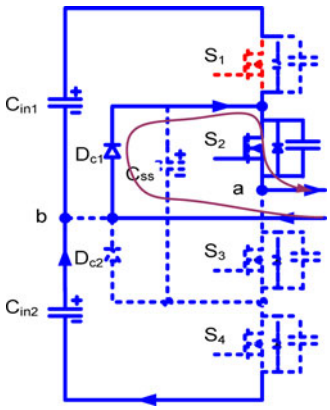

Fig. 9. S1 has an open circuit when S3 and S4 are OFF.

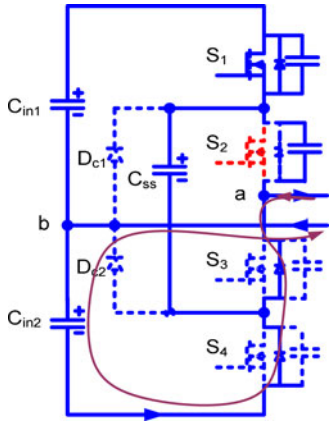

Fig. 10. S2 has an open circuit when S1 is ON.

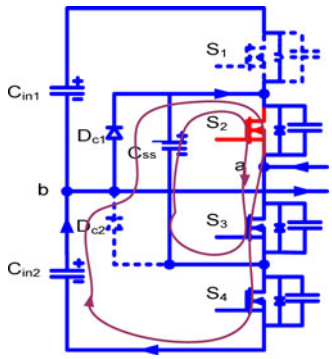

Fig. 11. S2 has a short circuit when S2 and S4 are ON.

the bottom input capacitor, Cin2, is continuously transferred to load when S3 and S4 are ON. However, when S3 and S4 are OFF and S2 turns ON, the upper input capacitor (Cin1) will be isolated because the upper clamping diode (Dc1) will provide a short-circuit loop for the inductor current, shown in Fig. 9. But the energy in the bottom input capacitor, Cin2, will gradually discharge to 0, as does Vcss. The transformer will be saturated soon due to negative biased dc voltage stress.

B. Outer Switch Short Circuit

If S1 has a short circuit, the flying capacitor will be directly connected with input power source when S3 and S4 are ON. Vcss is equal to full input voltage, as does S2. But the neutral point voltage would not be influenced by this fault.

C. Inner Switch Open Circuit

If S2 has an open-circuit fault, Vcss also increases to full input voltage soon. The mechanism is the same as the outer switch short-circuit case, i.e., both violate the rule that S1 has to turn OFF before S2 turns OFF. When S2 fails to open circuit, it means that S2 always turns OFF before S1 turns OFF. The Vcss increases to full input voltage through the S1 and the body diodes of S3 and S4, shown in Fig. 10. But the neutral voltage of input capacitor almost remains normal. The converter will stop delivering power to the load with this fault.

D. Inner Switch Short Circuit

If S2 has a short circuit, when S3 and S4 turn ON, the flying capacitor will be shorted through S2, and S3 and the bottom input capacitor Cin2 will be shorted through the upper clamping diode, S2, S3, and S4, shown in Fig. 11. Meanwhile, S1 has to withstand full input voltage when it is open. When S3 and S4 turn OFF, the fault does not effect the converter operation as usual and the flying capacitor and Cin2 will be charged back to half of the input voltage. Hence, the Vcss and neutral point voltage are pulses from zero to half of the input voltage with the same frequency as switching frequency. The transformer will be saturated soon due to the positive biased voltage stress.

E. Outer Switch Body Diode Open Circuit

If the switch S1's body diode D1 fails due to open circuit, this fault does not have any effect on the converter operation. As Fig. 12 shows, when S4 turns OFF and S3 is still ON, the inductor current will go through the bottom clamping diode back to the resonant tank instead of D1 after the S4's switch capacitor is charged to half of the input voltage and S1's switching is discharged to 0. Even if it is good, the D1 will never be conducted or involved in any commutation. The system is never affected by this fault. Certainly, this fault is undetectable by Vcss.

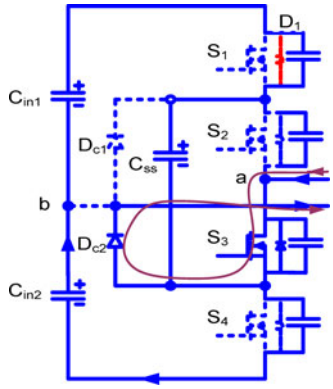

Fig. 12. D1 has an open circuit when S4 starts to turn OFF while S3 is still ON.

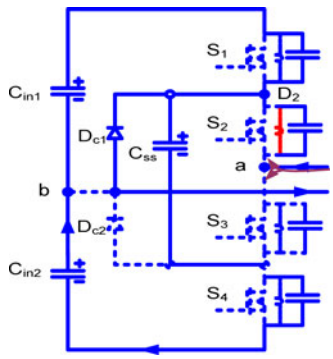

Fig. 13. D2 has an open circuit when S3 and S4 turn OFF.

F. Inner Switch Body Diode Open Circuit

If the switch S2's body diode D2 fails due to open circuit, the converter can work when the S1 and S2 are ON. When the S3 turns OFF after S4 turns OFF, the inductor current starts to charge the S3 switch capacitor and discharge the S2's switch capacitor. But the inductor current has no way to go after the S3's switch capacitor is charged to half of the input voltage and S2's switch capacitor is discharged to 0 due to the open circuit of D2, shown in Fig. 13. Therefore, S3 will suffer high voltage spike in this fault case. But the Vcss keeps the normal value. This fault cannot be detected unless the noise caused by high voltage spike triggers the protection. It is possible in practical application due to the high abnormal noise when ZVS is lost.

G. Clamping Diode Open Circuit

If the clamping diode Dc1 fails due to open circuit, the converter works normally if the converter is ideal. But the converter will practically lose the advantages of the three-level structure without the clamping diode. As long as the switch's voltage stresses are unbalanced, this fault will be detected by Vcss.

H. Clamping Diode Short Circuit

If the clamping diode Dc1 fails due to short circuit, the neutral point voltage will be connected with the positive polarity of the input voltage and charged to full input voltage when S1 is ON, so does flying capacitor. In this case, S1 suffers huge current when it is ON, or then S2 suffers over-voltage when it is OFF. Either one could fail before the neutral point voltage and Vcss reach the input voltage. Meanwhile, the transformer suffers a negative dc bias voltage.

I. Rectifier Diode Open circuit

If the rectifier diode Dr1 fails due to open circuit, no more energy will be transferred to the load when the resonant capacitor voltage is positive. But the converter keeps transferring the energy to the load when the resonant capacitor is negative. This unbalanced energy transfer will result in a positive dc biased voltage stress to the transformer. The neutral point voltage will decrease to 0 while the Vcss increases to the full input voltage. It should be noted that the neutral point voltage will increase if the rectifier diode in opposite bridge is open circuit while the Vcss still increases.

J. Rectifier Diode Short Circuit

If the rectifier diode Dr1 fails due to short circuit, the resonant capacitor will be shorted when the polarity of the resonant capacitor voltage is negative. More energy can be transferred to the transformer secondary side when S3 and S4 are ON. It follows that the neutral point voltage decreases and flying capacitor voltage increases. Same as Dr1 open-circuit fault case, the neutral point voltage will increase if the rectifier diode in opposite bridge is shorted while the Vcss still increases.

K. Load Open Circuit

If load open circuit happens, the output voltage will increase significantly due to the PRC inherent boost property. But the converter will operate normally except for high current when the switching frequency is higher than resonant frequency. Otherwise, the converter will lose ZVS operation and the fault will be detected by the increased Vcss.

L. Load Short Circuit

If load short circuit happens, the converter still keeps the ZVS mode due to the PRC property. Theoretically it cannot be detected by Vcss. But the turn-OFF current which depends on the switching frequency will increase due to the triangle current waveform. High voltage spike due to high turn-OFF current still may practically trigger the protection with Vcss detection.

The response of Vcss to load open circuit and load short circuit in this paper may vary in other three-level topologies because the inherent properties of PRC is dominated in these faults. Of all the possible contingencies, the protection against shoot-through is the trickiest one, and is very dependent on the parasitic inductance. In an ideal case, the voltages of the input capacitors and flying capacitors are equal to half of the input voltage without any parasitic inductance even during a shoot-through fault. However, since the input wire inductance of the power supply ($L_{\rm in}$) shown in Fig. 14 is usually very large or at least relatively larger than the parasitic inductance after the input capacitor as well as the relatively larger input capacitance, the Vcss will be dropped sharply as shoot-through happens.

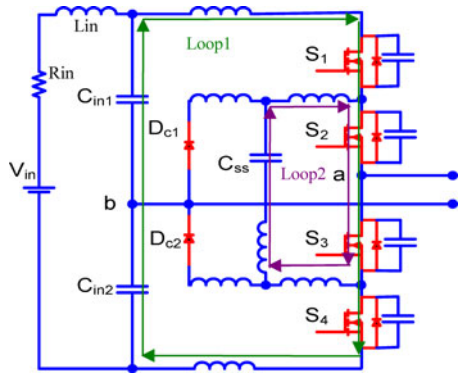

Fig. 14. Current loops as shoot-through occurs.

Fig. 14 shows two current loops during the initial time of shoot-through. In order to simplify the analysis, the following assumptions are made: First, the capacitance of the input capacitors is much larger than the flying capacitor. Second, the inductance in Loop 1 is much larger than the inductance in Loop 2 due to the large loop area. These two assumptions are reasonable in most cases due to the three-level structure and design requirements. Therefore, the Vcss instantly drops to 0 as the shoot-though increases, which is faster than the input capacitor voltage drop because the resonant frequency of Loop 1 is much lower than the resonant frequency of Loop 2. Detecting the shoot-through fault by Vcss drop instead of current sensor would not generate too much delay time.

In addition, considering the 10 μs short-circuit endurance time for IGBTs and the better short-circuit endurance of MOSFETs [29], the detection time is not an issue for Vcss detection based on the test, which is short enough to allow the controller to take related protective actions.

The analysis is verified with simulation in Saber. A three-level parallel resonant converter shown in Fig. 1 runs with the phase shift mode at 200 kHz. Each switch operates at nearly 50% duty cycle. The converter boosts 600 V input voltage to 10 kV load voltage. The main simulation waveforms are included in the Appendix. The simulation results are summarized in Table I where the abbreviations "ov" and "oc" are used to indicate the over-voltage and over-current. The phenomenon of Vcss may vary slightly with different three-level topologies and operation schemes due to the PRC characteristics. It should be noted that the undetectable cases mean that the voltage stresses are balanced based on the simulation with symmetrical parameters. Except for the fault case of D1 open circuit, all of the other undetectable cases may lose soft-switching or finally cause unbalanced voltage stresses, and then are detected by Vcss. In practice, the load short circuit fault is commonly protected by over-current protection.

IV. Design of Proposed Protection Circuit

For three-level structures, balance resistors are needed for the capacitors' voltage balance. Fig. 15 shows the connection of balance resistors. R_1 is equal to R_2, and R_3 is equal to R_6. In order to have half the input voltage, the sum of R_4 and R_5 is equal to the sum of R_3 and R_6. For a protection circuit, R_4 and R_5, with appropriate resistance, can be used as a voltage divider for the sensor of Vcss. For 600 V input voltage, 1 W 100 kΩ resistors with 1% tolerance are chosen for R_1, R_2, R_3 and R_6. R_4 is 198 kΩ and R_5 is 2 kΩ as a one hundredth voltage divider. The schematic of the proposed protection circuit is shown in Fig. 16. The sensed voltage is processed by a window detector with an isolated auxiliary power supply. The window detector output is transferred to the system controller through a high-speed optocoupler.

A. Flying Capacitor Design

Though the flying capacitor design is not directly related with the protection circuit design, the proposed protection method has to be based on the flying capacitor. In the conventional three-level converter with phase-shift control, the functions of the flying capacitor can be defined as follows:

1) decoupling the switching transitions of S1 and S4, S2 and S3;
2) balancing the unbalanced voltages between the two input capacitors;
3) acting as a snubber capacitor for inner switches, S2 and S3.

The decoupling effect is dependent upon on the ratio of capacitance, shown in the following:

$$\frac{V_{\rm css}}{V_{\rm sw}} = \frac{C_{\rm ss}}{C_{\rm sw}} \tag{3}$$

where $V_{\rm sw}$ is the minimum left voltage of any one of switches when its gate signal is becoming high during switching transition. ZVS is achieved when $V_{\rm sw}$ is near 0. $C_{\rm ss}$ is the capacitance of flying capacitor. $C_{\rm sw}$ is the sum of the capacitance of the switch capacitor and any external paralleled capacitor. For better decoupling and voltage clamping effect, the capacitance of the flying capacitor should be no less than the calculated number with (3).

Even if a phase shift control scheme is not employed and the flying capacitor is not necessary, the flying capacitor can still be added as a snubber capacitor and work for the proposed protection circuit.

B. Design Criteria

The Vcss is determined by the input voltage in steady-state operation. As the converter is running, the Vcss is mainly influenced by the voltage ripple of the input capacitors. Due to the clamping diode, the flying capacitor can be charged to the maximum voltage of the input capacitors, while the normal minimum Vcss is equal to the half of the low-line input voltage. So the high and low reference voltages have different considerations, and are expressed by (4) and (5)

$$V_{\rm ref\_H} = \frac{(1+k)}{2\cdot n} V_{\rm in\_high} \tag{4}$$

$$V_{\rm ref\_L} = \frac{V_{\rm in\_low}}{2\cdot n} \tag{5}$$

TABLE I
FAULT CASE STUDY WITH PHASE-SHIFT THREE-LEVEL PARALLEL RESONANT CONVERTER

Device / Fault Case	S1	S2	S3	S4	Dc1	Dc2	Results
S1 Open-circuit	ov				oc		*Vcss=0 gradually
S1 Short-circuit		ov	ov				*Vcss=Vin
S2 Open-circuit		ov	ov				*Vcss=Vin
S2 Short-circuit	ov		ov		oc	oc	*Vcss=0,Vin pulse
D1 Open-circuit							***No serious consequence
D2 Open-circuit		ov	ov				***S2 lose ZVS, S3 suffers huge voltage spike, Vcss=1/2Vin
Device / Fault Case	**S1**	**S2**	**S3**	**S4**	**Dc1**	**Dc2**	**Results**
Dc1 Open-circuit							***Have potential serious consequence*
Dc1 Short-circuit		ov	ov				*Vcss=Vin
Dr1 Open-circuit		ov	ov				*Vcss=Vin
Dr1 Short-circuit		ov	ov				*Vcss=Vin, OC for the other three rectifier diodes
Load Open-circuit	oc	ov oc	ov oc	oc			**Vcss=Vin if switching frequency is higher than resonant frequency, but Transformer secondary side components suffer high voltage.
Load Short-circuit							***Have potential serious consequence
Shoot-through	oc	oc	oc	oc			*Vcc drops.
* Detectable case			**Possible detectable case				***Undetectable case

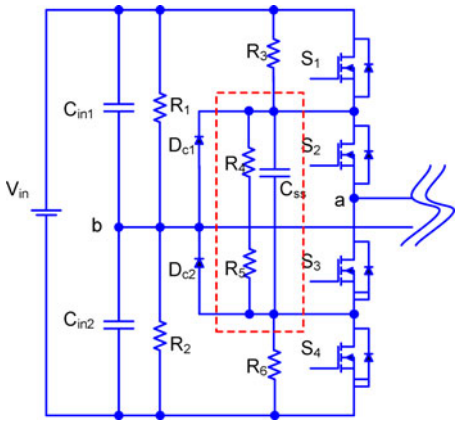

Fig. 15. Three-level structure with balance resistors.

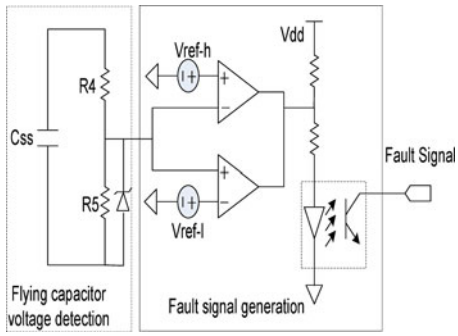

Fig. 16. Detection circuit through monitoring Vcss.

where $V_{\text{in\_high}}$ and $V_{\text{in\_low}}$ are the high-line input voltage and low-line input voltage, respectively; k is the allowed input capacitor voltage ripple defined in (2); and n is the ratio of the R_4/R_5 voltage divider.

Considering the dc signal on flying capacitor voltage, the detection signal is stable against noise and false trip can be avoided.

V. EXPERIMENTAL RESULTS

One of the real failures was successfully protected by the proposed protection and captured in our laboratory, and is shown in Fig. 17. A three-level parallel resonant converter was designed to supply 30 kW with 600 V dc input voltage and 200 kHz switching frequency. 600 V voltage rating MOSFET modules are used as main switches. The converter's key parameters are listed in Table II.

In Fig. 17, the transformer winding over-voltage breakdown results in secondary winding short circuit. The resonant capacitor is discharged to 0 suddenly, which is similar to the case of short circuit of one of rectifier diodes. The voltage stress of the

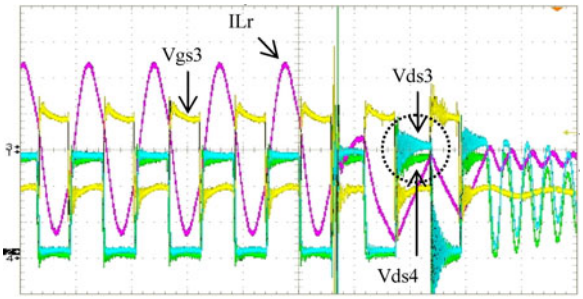

Fig. 17. System is protected by proposed protection when transform primary winding and secondary winding are voltage broken down. [Vgs3 (10 V/div),Vds3 (100 V/div), ILr (100 A/div), Vds4 (100 V/div), 2us/div].

TABLE II
CONVERTER'S KEY PARAMETERS

Parameters	Value
Transform turn ratio (secondary over primary)	11
Quality Factor (Q)	4
Voltage Gain (M)	3
Resonant Capacitor (Cp)	1.24 nF
Resonant Inductor (Ls)	3.63 μH
Flying capacitor (Css)	2 μF

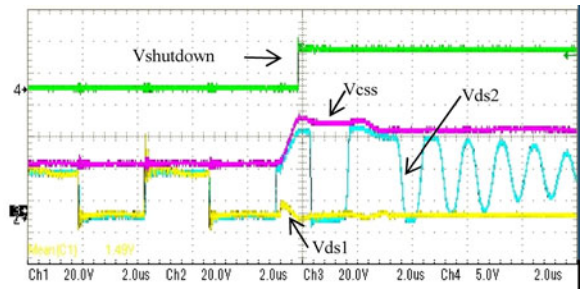

Fig. 18. Protection circuit against S1 short-circuit case [Vds1 (20 V/div), Vds2 (20 V/div), Vcss (20 V/div), Vshutdown (5 V/div), 2us/div].

inner switch, S3, immediately increases and is higher than the voltage stress of the outer switching, S4, which can be clearly observed in the dotted circle in Fig. 17. Based on previous analysis, the flying capacitor voltage is also abnormally increased. Therefore, the proposed protection is triggered and successfully protects the converter against the system failure. Note that as the transformer is broken down, the resonant capacitor voltage is discharged to 0. Thus, the resonant inductor current waveform in Fig. 17 becomes triangle waveform when the fault happens. In order to verify the analysis and the feasibility of the proposed protection, the scaled-down experiment is operated with 1/10th the input voltage and the same prototype.

Figs. 18–22 show the five selected faults respectively: S1 short circuit, S1 open circuit, S2 short circuit, S2 open circuit, and shoot-through. The fault conditions are generated by a timer and a fault signal. The converter enters the steady state before the end of timer. At the end of timer, a fault signal, low level pulse, is added into one of gate signals with a logic AND gate to simulate an open-circuit failure. If the fault signal is a high-level pulse, a short-circuit failure can be simulated when it is added into one of the gate signals through a logic OR gate. If the fault

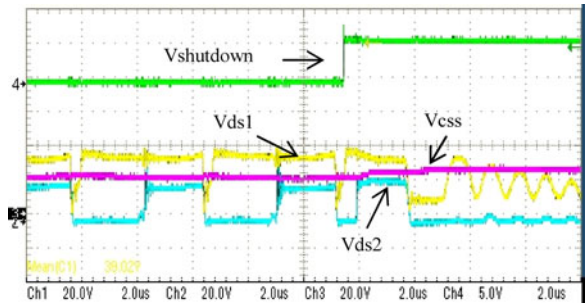

Fig. 19. Protection circuit against S1 open-circuit case [Vds1 (20 V/div), Vds2 (20 V/div), Vcss (20 V/div), Vshutdown (5 V/div), 2us/div].

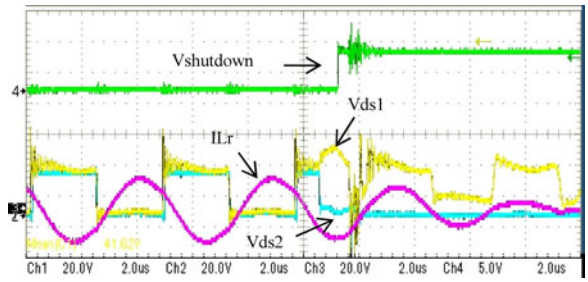

Fig. 20. Protection circuit against S2 short-circuit case [Vds1 (20 V/div), Vds2 (20 V/div), ILr (20 A/div), Vshutdown (5 V/div), 2us/div].

signal is added into all of the gate signals, shoot-through will happen. When the protection circuit is triggered, a shut-down signal (V shutdown) will be generated, which clears the fault signal and shuts down the system. The experimental results are consistent with the simulation analysis.

As S1 fails short circuit, as shown in Fig. 18, the voltage across inner switch S2 immediately increases to full input voltage, as well as the flying capacitor voltage. The first two cycles correspond to normal operation. The protection circuit is triggered in less than 1 μs, which is indicated by the shutdown signal.

As S1 fails open circuit, as shown in Fig. 19, the flying capacitor voltage gradually decreases, triggering the protection circuit. The fault had happened before the waveforms were captured. Compared with 30 V of Vcss and drain to source voltage of S2 (Vds2) at normal operation, the Vcss and Vds2 shown in Fig. 19 are about 20 V, which triggers the low-level limit of protection. The notch of the drain to source voltage of S1 (Vds1) waveform is due to the S1's body diode conduction. The clamping diode Dc1 has to withstand high conduction current when S2 turns ON.

Fig. 20 shows the S2 short-circuit case. The fault signal comes in the middle of the S2 OFF time while both bottom two switches (S3 and S4) are ON. The Vds1 quickly increases to full input voltage while the Vcss is discharged to zero and triggers the protection.

Fig. 21 shows the S2 open-circuit case. The fault signal comes before S2 and S1 are turned OFF. The Vcss starts to increase after the S2 fails to open circuit. Fortunately, soon it is time for the upper leg to turn OFF. Vcss keeps flat when S1 turns OFF. The notch of Vds2 is due to its body diode conduction during

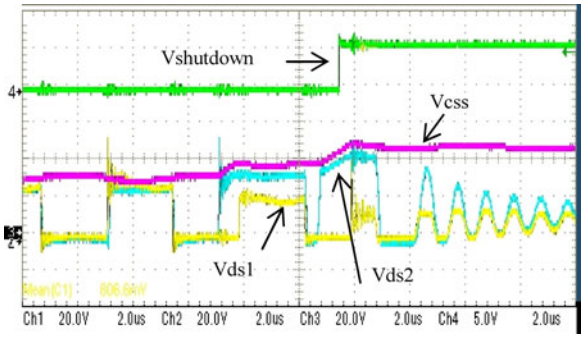

Fig. 21. Protection circuit against S2 open-circuit case [Vds1(20 V/div), Vds2 (20 V/div), Vcss (20 V/div), Vshutdown (5 V/div), 2us/div].

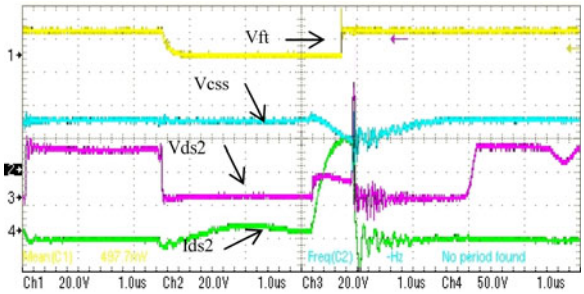

Fig. 22. Protection circuit against shoot-through [Fault trigger signal Vft (20 V/div), Vcss (20 V/div), Vds2 (20 V/div), Ids2 (50 A/div), 1 us/div].

the initial period when S1 turns ON again. When the inductor current changes the direction, the Vcss continues to increase, and then triggers the protection circuit.

The protection against shoot-through is shown in Fig. 22. The fastest response time is around 700 ns in this repeatable experiment for shoot-through fault.

VI. Conclusion

The proposed protection scheme based on flying capacitor voltage detection is presented in this paper. The reasons for the unbalanced voltage stress are categorized and illustrated in detail. Solutions to each unbalanced voltage stress are introduced. The possible faults are thoroughly analyzed and summarized in Table I. The proposed protection method can effectively avoid the device failure caused by unbalanced voltage stresses on switches in the three-level structure, and will protect the system even if a failure occurs. Remedies can be taken to prevent the consequent damages of the faults when the new protection method is employed. A detection circuit is proposed, and its design is addressed as well as flying capacitor selection. The theoretical analysis and simulation results are verified by experimental results. The protection scheme is very effective and reliable for three-level converter.

Appendix

In the following simulation waveforms, Vb is the neutral point voltage; Vgs1 is the gate voltage of switch S1; Vgs2 is the gate voltage of switch S2; the rest are the same as the definitions in paper.

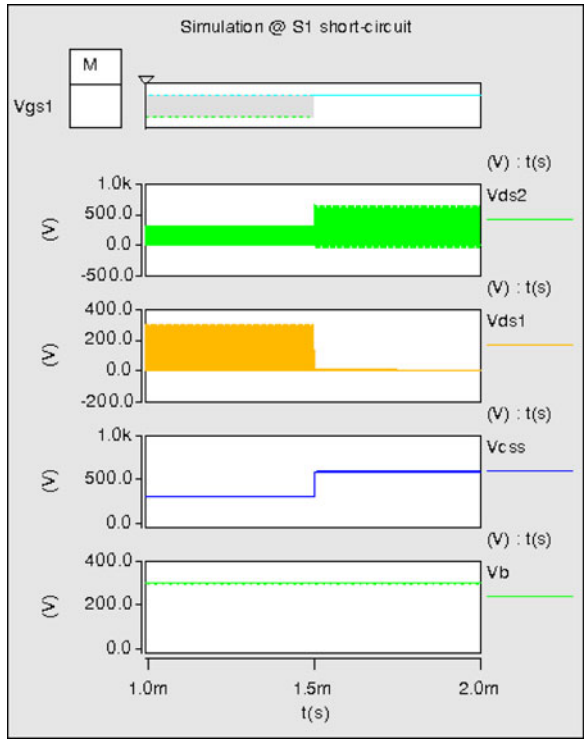

Fig. A1. Simulation with S1 short circuit.

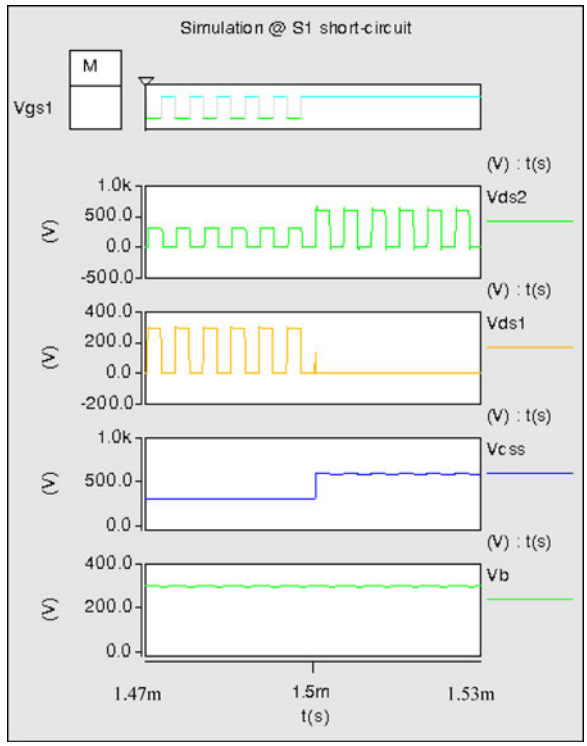

Fig. A2. Zoom-in of simulation with S1 shortcircuit.

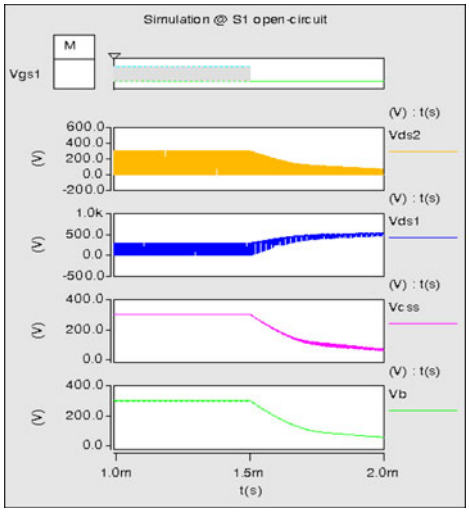

Fig. A3. Simulation with S1 open circuit.

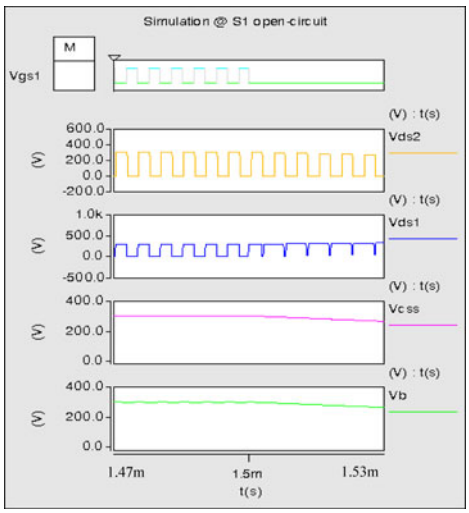

Fig. A4. Zoom-in of simulation with S1 open circuit.

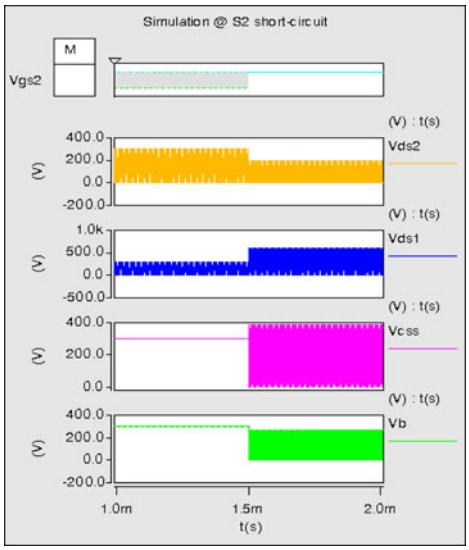

Fig. A5. Simulation with S2 short circuit.

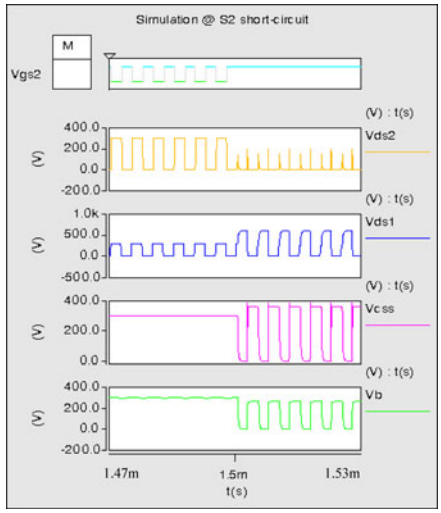

Fig. A6. Zoom-in of simulation with S2 short circuit.

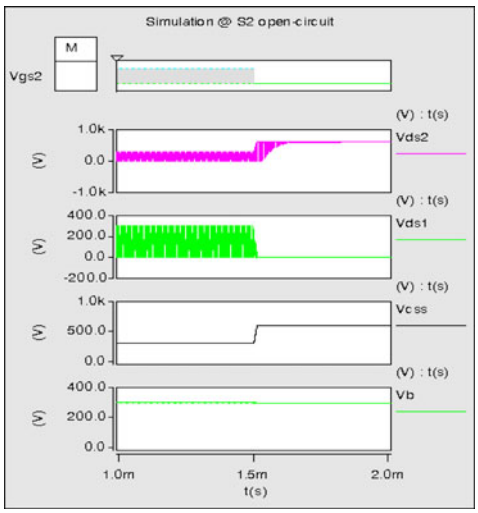

Fig. A7. Simulation with S2 open circuit.

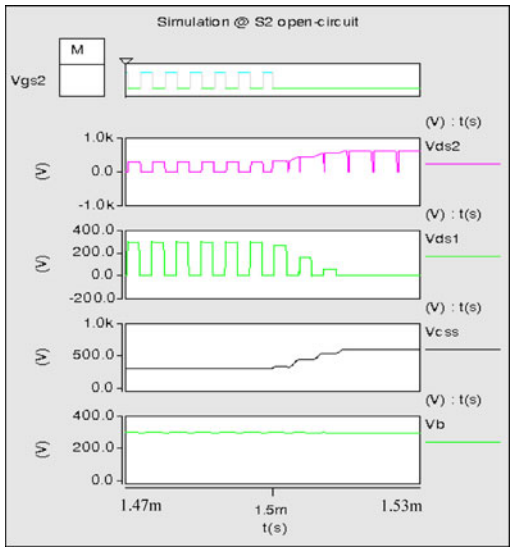

Fig. A8. Zoom-in of simulation with S2 open circuit.

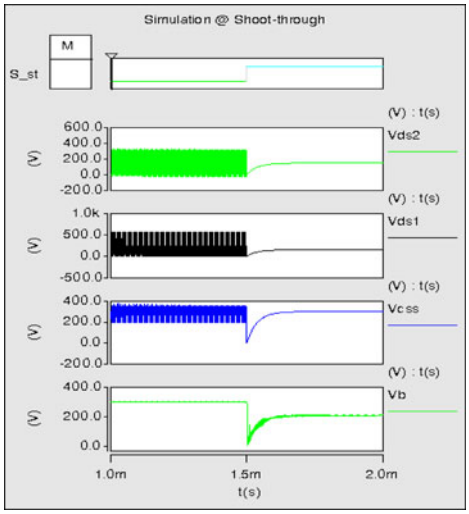

Fig. A9. Simulation with shoot-through case.

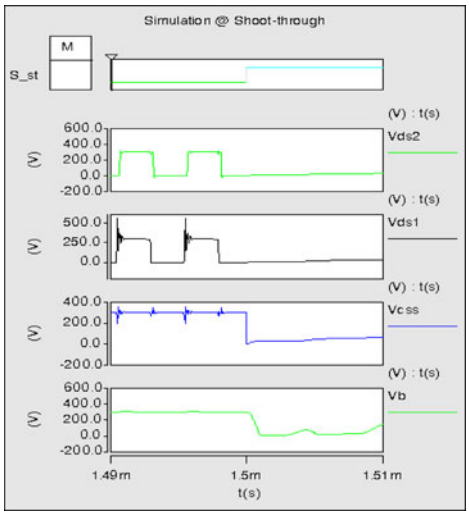

Fig. A10. Zoom-in of simulation with shoot-through case.

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Dr. Tipton is a senior member of the Power Components Branch, U.S. Army Research Laboratory (ARL), Adelphi, MD.