International Symposium on Low Power Electronics and Design 2007

August 27-29, 2007
Portland, Oregon, USA
Embassy Suites Portland Downtown
http://www.islped.org/

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Sunday August 26th

4:00PM-6:00PM Registration, Mezzanine

Monday August 27th

7:00AM-11:30AM and 1:00PM-5:00PM Registration, Mezzanine

7:00AM-8:15AM Breakfast

8:15AM-8:30AM Opening Address, Queen Marie Ballroom

General Chairs: Diana Marculescu (CMU) and Anand Raghunathan (NEC)

Program Chairs: Ali Keshavarzi (Intel) and Vijay Narayanan (PSU)

8:30AM-9:45AM Keynote, Queen Marie Ballroom

Robert Chau (Intel)

Nanotechnology for Low-Power and High-Speed Nanoelectronics Applications

9:30AM-9:45AM Break, Mezzanine

9:45AM-11:45AM Session 1

Queen Marie Ballroom

Emerging device technologies for low power

Chair: Yehia Massoud, Rice University, Co-chair: Chris Kim, University of Minnesota

1.1 Compact Modeling of Carbon Nanotube Transistor for Early Stage Process-Design Exploration (BEST PAPER NOMINEE)

Balijepallli, S. Sinha and Y. Cao, Arizona State University

1.2 A Floating-Body Dynamic Supply Boosting Technique for Low-Voltage PD/SOI CMOS SRAM

R. Joshi, R. Konj, K. Kim, R. Williams, C-T. Chuang, IBM Watson Research Center and IBM Austin Research Center

1.3 (s) Low Power FPGA Design Using Hybrid CMOS-NEMS Approach

Y. Zhou, S. Thekkel and S. Bhunia, Case Western University

1.4 (s) Design and Analysis of Thin-BOX FD/SOI Devices for Low-Power and Stable SRAM in sub-50nm Technologies

S. Mukhopadhyay, K. Kim and C-T. Chuang, IBM Watson Research Center

1.5 (s) Clocking structures and power analysis for nanomagnet-based logic devices

M. T. Niemier, X. S. Hu, M. Alam, G. Bernstein, W. Porod, M. Putney and J. DeAngelis, University of Notre Dame

9:45AM-11:45AM Session 2

Colonel Lindbergh Ballroom

Power-Efficient CMP Design

Chair: Massimo Poncino, Politecnico di Torino, Co-chair : Qing Wu, State Univ. of New York at Binghamton

2.1 Energy Efficient Near-threshold Chip Multi-processing (BEST PAPER NOMINEE)

B. Zhai, R. Dreslinski, D. Blaauw, T. Mudge and D. Sylvester, University of Michigan

2.2 Analysis of Dynamic Voltage/Frequency Scaling in Chip-Multiprocessors

S. Herbert and D. Marculescu, Carnegie Mellon University

2.3 (s) Evaluating Design Tradeoffs in On-Chip Power Management for CMPs

J. Sharkey, Assured Information Security Inc. A. Buyuktosunoglu and P. Bose, IBM Watson Research Center

2.4 (s) Impact of Die-to-Die and Within-Die Parameter Variations on the Throughput Distribution of Multi-Core Processors

K. Bowman, A. R. Alameldeen, S. T. Srinivasan ad C. B. Wilkerson, Intel

2.5 (s) A Reusability-Aware Cache Memory Sharing Technique for High-Performance Low-Power CMPs with Private L2 Caches

S. Youn, LG Electronics Inc. H. Kim and J. Kim, Seoul National University

11:45AM-1:15P Lunch, Arcadian Garden

1:15PM-3:15PM Session 3

Queen Marie Ballroom

Low-power Techniques for Logic, Clock Distribution, and Interconnect

Chair: Brian Otis, University of Washington , Co-chair : Saibal Mukhopadhay, IBM

1:15PM-3:15PM Session 4

Colonel Lindbergh Ballroom

Power Considerations at the physical level

Chair: Eli Chiprout, Intel, Co-chair : Azadeh Davoodi, University of Wisconsin

3.1 Dual Signal Frequencies and Voltage Levels for Low Power and Temperature-Gradient Tolerant Clock Distribution

S. A. Tawfik and V. Kursun, University of Wisconsin

3.2 A Robust Edge Encoding Technique for Energy-Efficient Multi-Cycle Interconnect

J. Seo, D. Sylvester, D. Blaauw, University of Michigan H. Kaul and R. Krishnamurthy. Intel

3.3 (s) Low Power Process Variation Tolerant Arithmetic Units Using Input Based Elastic Clocking

D. Mohapatra, G. Karakonstantis and K. Roy, Purdue University

3.4 (s) Sleep Transistor Sizing and Control for Resonant Supply Noise Damping

J. Gu, H. eom and C. H. Kim, University of Minnesota

3.5 (s) Thermal-Aware Methodology for Repeater Insertion in Low-Power VLSI Circuits

J. Ku and Y. Ismail, Northwestern University

4.1 Post-Placement Leakage Optimization for Partially Dynamic Reconfigurable FPGAs

C-F. Li, P-H. Yuh, C-L. Yang and Y-W. Chang, National Taiwan University

4.2 Power Optimal Repeater Insertion for Global Bus lines

H. Fatemi, B. Amelifard and M. Pedram, University of Southern California

4.3 (s) Timing Driven Row-Based Power Gating

A. Sathanur, A. Pullini, L. Benini*, A. Macii, E. Macii and M. Poncino, Politecnico di Torino and Univerista di Bologna*

4.4 (s) Detailed Placement for Leakage Reduction using Systematic Through-Pitch Variation

A. B. Kahng, Swamy Muddu, Puneet Sharma

University of California at San Diego

4.5 (s) Early power grid verification under circuit current uncertainties

I. A. Ferzli, F. Najm, University of Toronto L. Kruse, Magma Design Automation

3:15PM-3:30 PM Break, Mezzanine

3:30PM-5:00 PM Special Session, Queen Marie Ballroom

Shekhar Borkar (Intel) and William Dally (Stanford University)

On the future of on-chip interconnection architectures (NOCs and multi-cores)

5:00PM-6:30PM Session 5

Queen Marie Ballroom

Software and System Power Optimization

Chair: Joerg Henkel, University of Karlsruhe, Co-Chair: Yiran Chen, Seagate LLC

5.1 Towards a Software Approach to Mitigate Voltage Emergencies

M. S. Gupta, K. K. Rangan, M. D. Smith, G-Y Wei and D. Brooks, Harvard University

5.2 (s) Improving Disk Reuse for Reducing Power Consumption

M. Kandemir, S. Son The Pennsylvania State University M. Karakoy, Imperial College

5.3 (s) PVS: Passive Voltage Scaling for Wireless Sensor Networks

Y. Cho, Y. Kim and N. Chang, Seoul National University

5.4 (s) A Programming Environment with Runtime Energy Characterization for Energy-Aware Applications

C. Xian, Y-H. Lu and Z .Li, Purdue University

5:00PM-6:30PM Session 6

Colonel Lindbergh Ballroom

Leakage-Aware Architectural Synthesis

Chair: Ron Zhang, Qualcomm, Co-Chair: Yung-Hsiang Lu, Purdue University

6.1 A Process Variation Aware Low Power Synthesis Methodology for Fixed-point FIR filters

N. Banerjee, J. H. Choi, K. Roy, Purdue University

6.2 (s) Voltage - and ABB-Island Optimization in High Level Synthesis

D. Helms, O. Mayer, M. Hoyer and W. Nebel, OFFIS Research Institute and University of Oldenburg

6.3 (s) Power-Optimal RTL Arithmetic Unit Soft-Macro Selection Strategy for Leakage-Sensitive Technologies

S. Merdardoni, D. Bertozzi, University of Ferrara, E. Macii, Politecino di Torino

6.4 (s) Power Signal Processing: A New Perspective for Power Analysis and Optimization

Q. Zhou, L. Zhong and K. Mohanram, Rice University

6:30PM-7:30PM Reception, Wine Cellar

Tuesday August 28

7:00AM-11:30AM and 1:00PM-5:00PM Registration, Mezzanine

7:00AM-8:15AM Breakfast

8:15AM-10:15AM Session 7

Queen Marie Ballroom

Low-Power Memory Design and NBTI Detection

Chair: Gunjan Pandya, Intel, Co-chair: Volkan Kursun, University of Wisconsin

7.1 A 160 mV, Fully Differential, Robust Schmitt Trigger based Sub-threshold SRAM

J. P. Kulkarni, K. Kim. K. Roy, Purdue University

7.2 A Low-Power SRAM Using Bit-Line Charge-Recycling Technique

K. Kim, H. Mahmoodi*, K. Roy, Purdue University and San Francisco State University*

7.3 (s) Minimizing Power Dissipation during Write Operation to Register Files

K. Patel, W. Lee, M. Pedram, University of Southern California

7.4 (s) An On-Chip NBTI Sensor for Measuring PMOS Threshold Voltage Degradation

J. Keane, T-H. Kim, C. H. Kim, University of Minnesota

7.5 (s) Variable-latency Adder (VL-Adder): New Arithmetic Circuit Design Practice to Overcome NBTI

Y. Chen, H. Li, Seagate Technology. J. Li and C-K. Koh, Purdue University

8:15AM-10:15AM Session 8

Colonel Lindbergh Ballroom

DVS and thermal management

Chair: Z. Lu, Marvell Semiconductors, Co-chair :Jun Yang, Univ. of Pittsburgh

8.1 Throughput of multi-core processors under thermal constraints

R. Rao, S. Vrudhula, C. Chakrabartu, Arizona State University

8.2 Dynamic Voltage Frequency Scaling for Multi-tasking Systems Using Online Learning

G. Dhiman and T. Rosing, University of California, San Diego

8.3 (s) Thermal-aware Task Scheduling at the System Software Level

J. Choi, C-Y. Cher, H. Franke, H. Hamann, A. Weger, P. Bose, IBM Watson Research Center

8.4 (s) Thermal Response to DVFS: Analysis with an Intel Pentium M

H. Hanson, S. W. Keckler, The University of Texas at Austin. S. Ghiasi, K. Rajamani, F. Rawson, J. Rubio, IBM Austin Research Laboratory

8.5 (s) Approximation Algorithms for Power Minimization of Earliest Deadline First and Rate Monotonic Schedules

S. Zhang, K. S. Chatha and G. Konjevod, Arizona State University

10:15AM-10:30AM Break, Mezzanine

10:30AM-11:30AM Plenary Speech, Queen Marie Ballroom

David Patterson (UC Berkeley)

The Parallel Computing Landscape: A Berkeley View

11:30AM-1:00PM Lunch, Arcadian Garden

1:00PM-3:00PM Session 9

Queen Marie Ballroom

Signal Processing, Wireless, and Communication

Chair: Chaitali Chakrabarti, Arizona State University, Co-chair : Farzan Fallah, Fujitsu Labs

9.1 Low Power Soft-Output Signal Detector Design for Wireless MIMO Communication Systems (BEST PAPER NOMINEE)

S. Chen and T. Zhang, Rensselaer Polytechnic Institute

9.2 A Low Power Multimedia SoC with Fully

1:00PM-3:00PM Session 10

Colonel Lindbergh Ballroom

Architectural Power Optimization

Chair: Geoffrey Yeap, Qualcomm, Co-chair : Yu Cao, Arizona State University

10.1 A 0.4-V UWB Baseband Processor (BEST PAPER NOMINEE)

V. Sze and A. P. Chandrakasan, MIT

10.2 Resource Area Dilation to Reduce Power Density in Throughput Servers

M. D. Powell, Intel, T N Vijaykumar, Purdue

Programmable 3D Graphics and MPEG4/H.264/JPEG for Mobile Devices

J-H Woo, J-H Sohn, H. Kim, J. Jeong*, E. Jeong*, S. J. Lee* and H-J. Yoo, KAIST and *Corelogic, Inc.

9.3 (s) An Architecture for Energy Efficient Sphere Decoding

R. Jenkal and R. Davis, North Carolina State University

9.4 (s) On the Selection of Arithmetic Unit Structure in Voltage Overscaled Soft Digital Signal Processing

Y. Liu and T. Zhang, Rensselaer Polytechnic Institute

9.5 (s) Low-power H.264/AVC Baseline Decoder for Portable Applications

K. Xu and C. S. Choy, The Chinese University of Hong Kong

University

10.3 Locality Driven Architectural Cache Sub-Banking for Leakage Energy Reduction

O. Golubeva, M. Loghi, E. Macii, M. Poncino, Politecino di Torino

10.4 A Multi-Model Power Estimation Engine for Accuracy Optimization

F. Klein, G. Araujo, R. Azevedo, UNICAMP, Brazil R. Leao, L. C. V. dos Santos, UFSC

3 :00PM-3:15PM Break, Mezzanine

3 :15PM-4:30PM Embedded Tutorial: Queen Marie Ballroom

Ultra-Low Power Digital Techniques

Vojin Oklobdzija (UC Davis), Victor Zyuban (IBM)

4 :30PM-5:30PM Design Contest and Industry Sessions, Colonel Lindbergh Ballroom and Queen Marie Ballroom

6:30PM-9:00PM Dinner and Banquet, Willamette River Cruise and Dinner

Wednesday August 29th

7:00AM-10:30AM Registration, Mezzanine

7:00AM-8:00AM Breakfast

8:00AM-10:00AM Session 11
Queen Marie Ballroom

DC/DC Converters

Chair: William Li, Intel, Co-chair : Domine Leenaerts, NXP

11.1 A Fast-Transient Over-Sampled Delta-Sigma Adaptrive DC-DC Converter for Power-Efficient Noise-Sensitive Devices

M. Song and D. Ma, University of Arizona

11.2 High-efficiency Synchronous Dual-output Switched Capacitor DC/DC Converter with Digital State Machine Control

H. Shiming, W. Xiaobo, Zhejiang University. L. Yang, Analog Devices, Inc.

11.3 (s) A Micro power management system and maximum output power control for solar energy harvesting applications

H. Shao, C-Y Tsui and W-H Ki, The Hong Kong University of Science and Technology

11.4 (s) Advanced thermal sensing circuit and test techniques used in a high performance 65nm processor

D. E. Duarte, G. Taylor, K. L. Wong, U. Mughal, G. Geannopoulos, Intel

11.5 (s) Single inductor, Multiple Input, Multiple Output (SIMIMO) Power Mixer-Charger-Supply System

M. Chen and G. A. Rincón-Mora, Georgia Tech

8:00AM-10:00AM Session 12
Colonel Lindbergh Ballroom

Energy and Power Delivery

Chair: Nemani Mahadev, Intel, Co-chair : Swarup Bhunia, Case Western University

12.1 Vibration energy scavenging and management for ultra low power applications (BEST PAPER NOMINEE)

L. Chao, C-Y Tsui and W-H Ki, The Hong Kong University of Science and Technology

12. 2 Energy management of DVS-DPM enabled embedded systems powered by fuel cell-battery hybrid source

J. Zhou, C. Chakrabarti, Arizona State University, N. Chang, Seoul National University

12.3 (s) Design of an Efficient Power Delivery Network in an SoC to Enable Dynamic Power Management

B. Amelifard and M. Pedram, University of Southern California

12.4 (s) Energy-Efficient and Performance-Enhanced Disks Using Flash-Memory Cache

J-W. Hsieh, National Chiayi University, T-W. Kuo, P-L. Wu, National Taiwan University, Y-C. Huang, Genesys Logic Inc.

12.5 (s) SAPP: Scalable and Adaptable Peak Power Management in NoCs

P. S. Bhojwani, J. D. Lee and R. N. Mahapatra, Texas A & M University

10:00AM-10:15AM Break, Mezzanine

10:15AM-11:15AM Plenary Speech, Queen Marie Ballroom

Luiz Barroso (Google)

All Watts Considered

11:15AM-12:45PM Poster Session, Posters in Mezzanine, Presentations in Colonel Lindbergh Ballroom

Chair: A. Shrivastava, Arizona State University

1. Electromigration and Voltage Drop Aware Power Grid Optimization for Power Gated ICs

   Aida Todri (UCSB), Shih-Chieh Chang (NTHU), Malgorzata Marek-Sadowska (UCSB)
2. Power-Efficient LDPC Code Decoder Architecture

   Kazunori Shimizu (Waseda University), Nozomu Togawa (Waseda University), Takeshi Ikenaga (Waseda University), Satoshi Goto (Waseda University)
3. Adaptive Analog Biasing - A Robustness-Enhanced Low-Power Technique for Analog Baseband Design

   Zhenhua Wang (NXP Semiconductors)
4. Slope Interconnect Effort: Gate-Interconnect Interdependent Delay Model

Myeong-Eun Hwang (Purdue University)

5. Signoff Power Methodology for Contactless Smartcards
   Julien MERCIER (STMicroelectronics), Christian DUFAZA (L2MP - Univ. Provence), Mathieu LISART (STMicroelectronics)
6. Power-Aware Operand Delivery
   Erika Gunadi (University of Wisconsin - Madison), Mikko H. Lipasti (University of Wisconsin - Madison)
7. Reducing Display Power in DVS-enabled Handheld Systems
   Jung-hi Min (Yonsei University), Hojung Cha (Yonsei University)
8. Reducing Cache Power by Tag Encoding in Embedded Processors
   Mingming Zhang (Institute of Computing Technology, Chinese Academy of Sciences), Xiaotao Chang (Institute of Computing Technology, Chinese Academy of Sciences), Zhimin Zhang (Institute of Computing Technology, Chinese Academy of Sciences)
9. A methodology for analysis and verification of power gated circuits and designs with correlated results
   Aveek Sarkar (Apache Design Solutions), Shen Lin (Apache Design Solutions), Kai Wang (Apache Design Solutions)
10. Multicasting based Topology Generation and Core Mapping for a Power Efficient Networks-on-Chip
    Balasubramanian Sethuraman (University of Cincinnati), Ranga Vemuri (University of Cincinnati)
11. A 65-nm Pulsed Latch with a Single Clocked Transistor
    Martin Saint-Laurent (Qualcomm), Baker Mohammad (Qualcomm), Paul Bassett (Qualcomm)
12. On Reducing Energy Consumption by Late-Inserting Instructions into the Issue Queue
    Enric Morancho (DAC-UPC), Jose M. Llabería (DAC-UPC), Àngel Olivé (DAC-UPC)
13. On the Latency, Energy and Area of Checkpointed, Superscalar Register Alias Tables
    Elham Safi (University of Toronto), Patrick Akl (University of Toronto), Andreas Moshovos (University of Toronto), Andreas Veneris (University of Toronto)
14. A Low-Power CSCD Asynchronous Viterbi Decoder for Wireless Applications
    Mohamed Kawokgy (University of Toronto), C. André T. Salama (University of Toronto)
15. Phase-aware Adaptive Hardware Selection for Power-efficient Scientific Computations
    Konrad Malkowski (The Pennsylvania State University), Mahmut Kandemir (ThePennsylvania State University), Padma Raghavan (The Pennsylvania State University), Mary Jane Irwin (The Pennsylvania State University)
16. An ILP Based Approach to Reducing Energy Consumption in NoC Based CMPs
    Ozcan Ozturk (PSU), Mahmut Kandemir (PSU), S.-W. Son (PSU)
17. VT Balancing and Device Sizing Towards High Yield of Sub-threshold Static Logic Gates
    Yu Pu (Eindhoven University of Technology), José Pineda de Gyvez (NXP Research), Henk Corporaal (Eindhoven University of Technology), Yajun Ha (National University of Singapore)

12:45PM-1:00PM Conference Closing Session, Colonel Lindbergh Ballroom

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