General Description

The evaluation kit demonstrates the performance and features of the AT1201. The kit provides several methods for generating data from the ADC including PCM outputs through the natively generated I^S or LJ streams, as well as using an on-board DIT to provide AES compliant output through an XLR interface, an electrical S/PDIF interface, and an optical S/PDIF interface.

The multibit modulator outputs and DSD outputs are available through headers on the board for interfacing to data acquisition equipment, an FPGA board, or a DSP.
Testing the AT1201EVK
This section describes the test setup for the evaluation board.

Items Needed
1. AT1201 Evaluation Board Rev. 3.0
2. Rohde & Schwarz UPV, Audio Precision SYS-2722 or equivalent Audio Analyzer
3. Power supplies for +6V and ±8V and power cables
4. Two XLR male to female cables to connect signal generators to the board
5. An XLR cable, an S/PDIF optical cable, an RCA cable, or a 10-pin header with a ribbon
cable to connect ADC outputs to the analyzer.

Audio Interfaces and Supported Sampling Rates
Some audio interfaces have speed limitations that prevent them from supporting certain audio
sampling rates. The following table shows the rates supported by each interface.

<table>
<thead>
<tr>
<th></th>
<th>AES</th>
<th>S/PDIF Optical</th>
<th>S/PDIF RCA</th>
<th>I2S</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single: 44.1/48 kHz</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Dual: 88.2/96 kHz</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Quad: 176.4/192 kHz</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Octal: 352.8/384 kHz</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>Y</td>
</tr>
</tbody>
</table>

Table 1: Sampling Rates Supported by Various Interface Standards

The I2S interface has been tested successfully at 384 kHz using a Rohde & Schwarz UPV with the
optional I2S plug-in card.
Evaluation Board Overview

Test Procedure for PCM Output
1. Connect signal generators to analog inputs (J1 and J2) with XLR cables. The input buffers are configured such that full scale input corresponds to approximately 11V or +23dBu.
2. Connect the desired output to the signal analyzer. The EVK provides an S/PDIF Optical output. It can additionally be configured for either the AES output or the S/PDIF RCA output. To use AES XLR output, remove any jumpers from J13. To make the S/PDIF RCA output functional, you must place two jumpers vertically in J13.
3. Connect +6V, +8V and -8V power supplies.
4. Set the sampling rate as shown below in SW3 for the AT1201

<table>
<thead>
<tr>
<th>Mode</th>
<th>SW3:10 - M1</th>
<th>SW3:9 - M0</th>
<th>SW3:6 - MDIV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Double</td>
<td>Low</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Quad</td>
<td>High</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Octal</td>
<td>High</td>
<td>High</td>
<td>Low</td>
</tr>
</tbody>
</table>

5. Set the sampling rate as shown below in SW4 for the Digital Audio Transmitter

<table>
<thead>
<tr>
<th>Mode</th>
<th>SW4:2 - DITCK1</th>
<th>SW4:1 - DITCK0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Double</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Quad</td>
<td>Low</td>
<td>Low</td>
</tr>
</tbody>
</table>

6. Other settings for SW3/SW4/SW5 switches

<table>
<thead>
<tr>
<th>Switch</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW3:1</td>
<td>CLK22M</td>
<td>Enables crystal oscillator Y1</td>
</tr>
<tr>
<td>SW3:2</td>
<td>CLK24M</td>
<td>Enables crystal oscillator Y2</td>
</tr>
<tr>
<td>SW3:3</td>
<td>CLK24M</td>
<td>Enables crystal oscillator Y2</td>
</tr>
<tr>
<td>SW3:7</td>
<td>HPF_B</td>
<td>0: enable high pass filter 1: disable high pass filter</td>
</tr>
<tr>
<td>SW3:8</td>
<td>CLKEXT</td>
<td>Enables external MCLK clock input</td>
</tr>
<tr>
<td>SW3:9</td>
<td>I2S_LJ</td>
<td>0: left justified PCM output 1: i2S PCM output</td>
</tr>
<tr>
<td>SW4:5</td>
<td>MS</td>
<td>0: PCM slave mode 1: PCM master mode</td>
</tr>
<tr>
<td>SW4:6</td>
<td>DSD_EN</td>
<td>0: disable DSD outputs 1: enable DSD outputs</td>
</tr>
<tr>
<td>SW4:7</td>
<td>MBO_EN</td>
<td>0: disable multibit outputs 1: enable multibit outputs</td>
</tr>
<tr>
<td>SW4:8</td>
<td>PCM_EN</td>
<td>0: disable PCM outputs 1: enable PCM outputs</td>
</tr>
<tr>
<td>SW5:8</td>
<td>VCXO48K</td>
<td>Enables 48 kHz-base VCXO</td>
</tr>
<tr>
<td>SW5:9</td>
<td>VCXO44K1</td>
<td>Enables 44.1 kHz-base VCXO</td>
</tr>
<tr>
<td>SW5:10</td>
<td>EXTWC</td>
<td>Enables external WCLK clock input</td>
</tr>
</tbody>
</table>

7. Press the ADC reset push button followed by the DIT reset push button. The current draw should be approximately 210mA from the +6V supply and 50mA from the ±8V supplies. Note that power consumption is sampling rate and audio interface dependent.

8. Repeat the reset procedure after each mode change.
Clocking Modes
The AT1201EVK supports several mechanisms for providing a master clock to the device under test: an external MCLK clock via BNC connector J7, on-board crystal oscillators Y1 and Y2, and an optional phase-locked loop, which may be specified at the time of ordering. Source selection is performed by using switches SW3:1..3 to select each of the MCLK sources, respectively. Note that only one of these switches should be in the HIGH position at any time, and SW5:10 should be in the LOW position as well. By default, the evaluation kit comes with a 24.576 MHz crystal oscillator in position Y2 and no PLL oscillator.

The default 24.576 MHz crystal oscillator provides an on-board low jitter source for operating the AT1201 at 48 kHz, 96 kHz, 192 kHz, and 384 kHz PCM modes in addition to MBO and DSD modes. For clock rates at multiples of 44.1 kHz, an oscillator can be added at position Y1; this is also available upon request from Arda.

PLL configuration
If your EVK is supplied with a phase-locked loop VCXO, it can be used by introducing a base-rate (PCM mode) clock at the BNC connector, choosing the desired VCXO at SW5:8 or 9, and enabling the external clock using SW5:10. The three MCLK sources at SW4 should be disabled, and only one VCXO should be enabled at a time. The clock supplied to the BNC input should be within approximately 200 ppm above or below the desired base rate, and the AT1201 must have PCM mode enabled (SW4:8 HIGH) and be in Master mode (SW4:5 HIGH) for the PLL to lock. DSD and MBO modes can also be used, though the MCLK is supplied by the EVK and locking to an external MCLK is not supported.

Overflow
The overflow indicator output from the IC carries overflow information for both channels as a time multiplexed signal. The indicator drives an LED directly and is demuxed to drive two other LEDs representing each channel.

Buffer Gain & Bandwidth
The analog input buffers, U2 and U3, have been designed for a 110 kHz -3dB, single pole roll-off. The buffer bandwidth can be altered by changing passives around the operational amplifiers. This is a complicated process that can have a significant impact on the performance of the DUT. Arda Technologies will provide assistance if a different bandwidth is desired.

The signal gain through the input buffers is approximately 0.3 V/V, making the full-scale input level +23dBu. As with the buffer bandwidth, the gain can be altered by changing passives. Arda Technologies will provide assistance if a different gain is desired.

Digital Highpass Filter
A first-order IIR highpass filter is present in the PCM signal path. The -3dB frequency is 0.47Hz at Fs = 48kHz and scales with Fs. The filter is activated using SW3:7.

The highpass filter can be turned on for a few seconds to acquire the signal path offset and then disabled. Once disabled, the offset continues to be subtracted from the signal, but the filter’s frequency response is no longer present. Alternatively, the filter can be left enabled to operate continuously.
Test Procedure for DSD and MBO Outputs
Multibit and DSD outputs are available on the evaluation board. To activate these outputs, the MBO_EN or the DSD_EN signals must first be set high in SW4.

The MBR5 .. MBR0 and MBL5 .. MBL0 outputs, corresponding to the right and left channels, respectively, begin to toggle when the MBO_EN signal is high. Bit 5 is the MSB, and bit 0 is the LSB. These logic signals must be clocked on the rising edge of the DCLK output from the DUT.

The DSDR and DSDL outputs, corresponding to the right and left channels, respectively, are activated when the DSD_EN signal is high. They must be clocked on the rising edge of the DCLK output from the DUT.

Board Schematics and Layout
Evaluation board schematics are illustrated on the following pages. Gerber files for the board layout are available on request.

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Typical Measured Performance

The following plots show typical measured performance for the AT1201 operating in the Evaluation Kit.

Unless otherwise noted, AVDD = 5.0V, DVDD = 3.3V, 1 kHz test tone.

Figure 1: THDN vs Amplitude
Figure 2: Level THDN vs Amplitude
Figure 3: THD vs Amplitude
Figure 4: THDN vs Frequency

Operating level: -2 dB FS
Figure 5: Intermodulation

Tones: 17997 Hz and 18997 Hz at -16 dB FS
Figure 6: Interchannel Isolation

Channel 1 driven at -1 dB FS, channel 2 undriven. Output of channel 2 displayed.
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