Ultra High Performance Audio ADC
124dB, 384kHz, 24-Bit Conversion

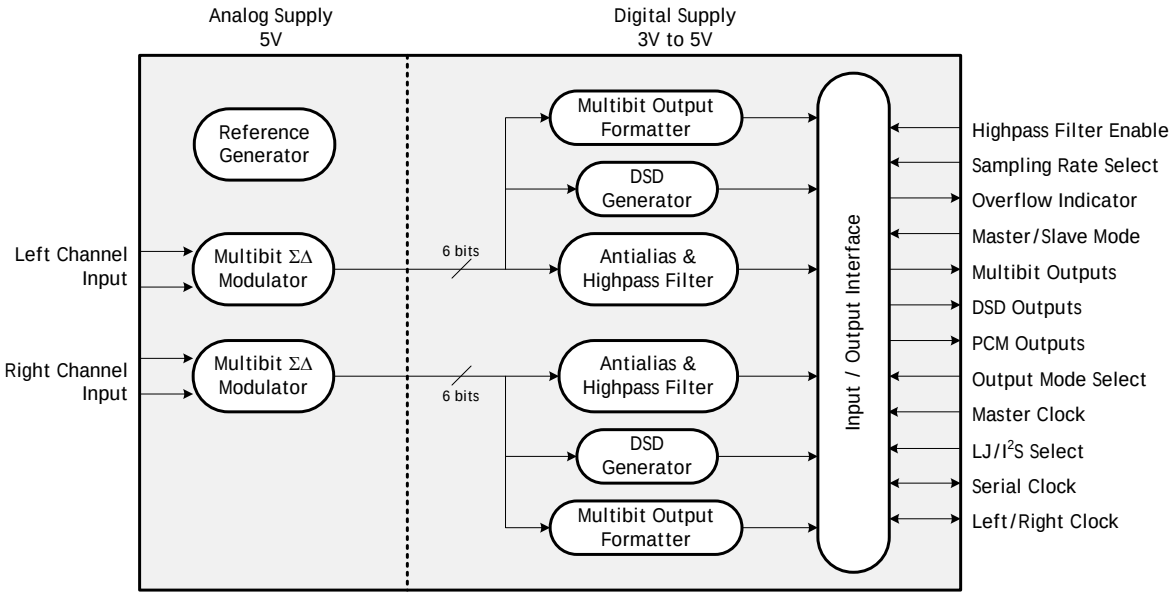
Datasheet AT1201

Features

- Dynamic Range: 124dB
- THD+N: -105dB
- Sampling Frequency: up to 384kS/s
- PCM formats: I²S™, Left justified
- Multibit and DSD outputs
- Lowest Group Delay Filter
- Digital High Pass & Offset Cancellation
- Overflow Indicator
- Supports Logic Levels from 3.3V to 5V
- Power dissipation: 696mW
- QFN-64 Green Package, 9mm x 9mm

Applications

- High Performance Audio
- Digital Audio Mixing Consoles
- Live Sound Production
- Surround Sound Encoders
- Effects Processors
- Broadcast Studio Equipment
- A/V Receivers
- DVD-R, CD-R
- Data Acquisition and Test Equipment

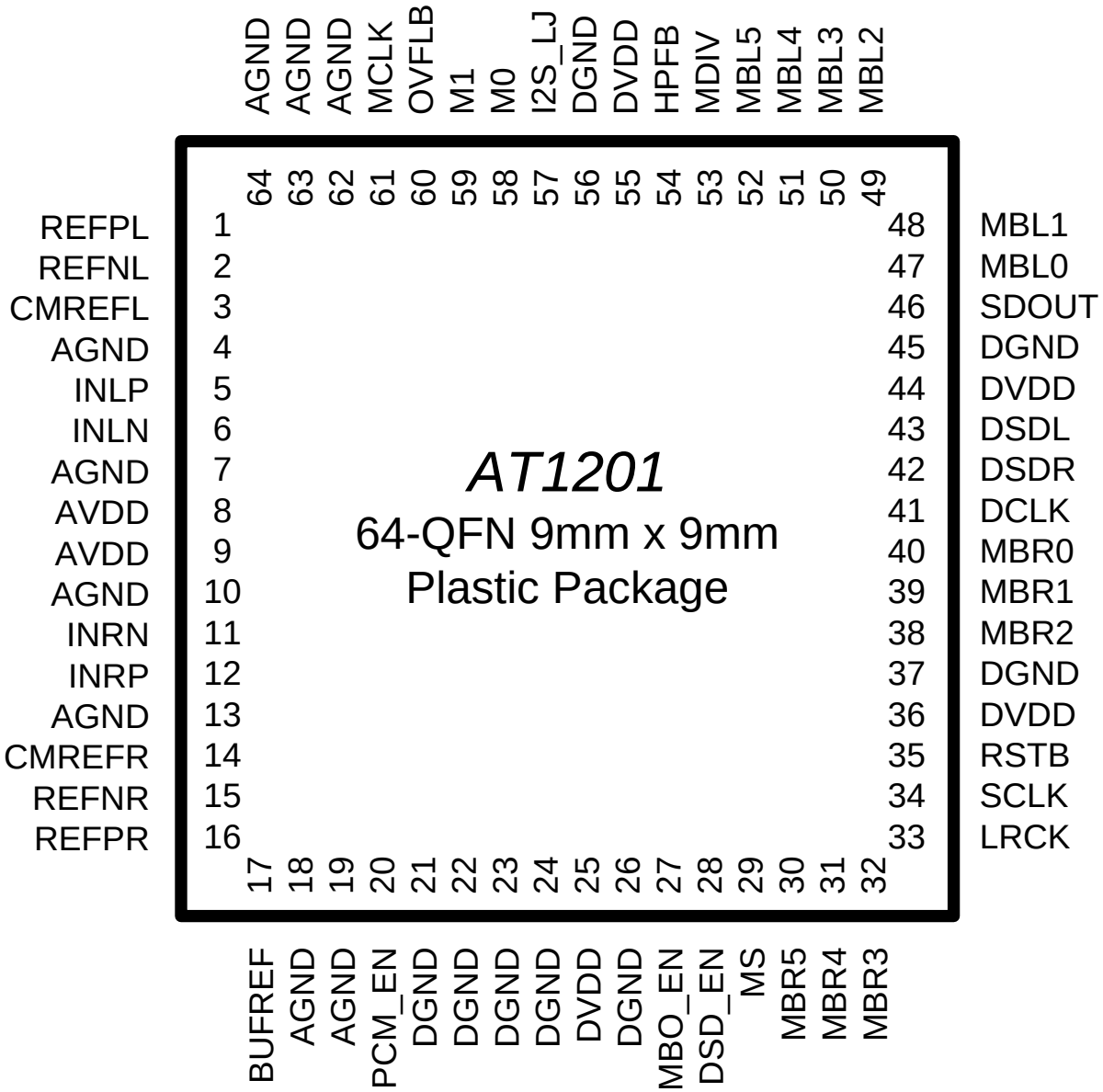


General Description

The AT1201 is a stereo A/D converter designed for the most uncompromising high performance audio systems. Using a proprietary multibit sigma-delta modulator architecture, the AT1201 provides the industry's highest dynamic range of 124dB, excellent THD+N of -105dB and a sampling rate of up to 384kS/s.

On-chip digital filters are designed for sonically transparent response in all four sampling rate modes. Multibit modulator and DSD outputs enable the use of external filters, and all three output modes (PCM, DSD, and multibit) can be enabled simultaneously.

Pinout


AT1201
64-QFN 9mm x 9mm
Plastic Package
1 REFPL
2 REFNL
3 CMREFL
4 AGND
5 INLP
6 INLN
7 AGND
8 AVDD
9 AVDD
10 AGND
11 INRN
12 INRP
13 AGND
14 CMREFR
15 REFNR
16 REFPR
17 BUFREF
18 AGND
19 AGND
20 PCM_EN
21 DGND
22 DGND
23 DGND
24 DGND
25 DVDD
26 DGND
27 MBO_EN
28 DSD_EN
29 MS
30 MBR5
31 MBR4
32 MBR3
33 LRCK
34 SCLK
35 RSTB
36 DVDD
37 DGND
38 MBR2
39 MBR1
40 MBR0
41 DCLK
42 DSDR
43 DSDL
44 DVDD
45 DGND
46 SDOUT
47 MBL0
48 MBL1
49 MBL2
50 MBL3
51 MBL4
52 MBL5
53 MDIV
54 HPFB
55 DVDD
56 DGND
57 I2S_LJ
58 M0
59 M1
60 OVFLB
61 MCLK
62 AGND
63 AGND
64 AGND

1. Pin Description

Terminal No.	Terminal Name	Type	Pin Description
1	REFPL	Analog Input	**High Reference Left Channel** – High reference voltage for left channel, ties to capacitor
2	REFNL	Analog Input	**Low Reference Left Channel** – Low reference voltage for left channel, ties to analog ground
3	CMREFL	Analog Output	**Common-Mode Voltage** - Internally generated reference voltage, ties to capacitor
4, 7, 10, 13, 18, 19, 62, 63, 64	AGND	Analog Ground	**Analog Ground** – Ground return for analog section
5	INLP	Analog Input	**Differential Left Channel Input** – Differential analog input to the left channel ΣΔ modulator
6	INLN		
8, 9	AVDD	Analog Supply	**Analog Power** – Positive power supply for analog section
11	INRN	Analog Input	**Differential Right Channel Input** – Differential analog input to the right channel ΣΔ modulator
12	INRP		
14	CMREFR	Analog Output	**Common-Mode Voltage** - Internally generated reference voltage, ties to capacitor
15	REFNR	Analog Input	**Low Reference Right Channel** – Low reference voltage for right channel, ties to analog ground
16	REFPR	Analog Input	**High Reference Right Channel** – High reference voltage for right channel, ties to capacitor
17	BUFREF	Analog Output	**Input Buffer Common-Mode Reference Voltage** – Reference voltage for the buffers driving the analog inputs
20	PCM_EN	Digital Input	**Enable PCM Output** – Enables internal filters and generates serial audio output
21, 22, 23, 24, 26, 37, 45, 56	DGND	Digital Ground	**Digital Ground** – Ground return for digital section
25, 36, 44, 55	DVDD	Digital Supply	**Digital Power** – Positive power supply for digital section
27	MBO_EN	Digital Input	**Multibit Modulator Output Enable** – Enables right and left channel multibit modulator outputs
28	DSD_EN	Digital Input	**DSD Output Enable** – Enables right and left channel DSD outputs
29	MS	Digital Input	**Master/Slave mode** – Selects clock master or clock slave mode for PCM output, high=master / low=slave
30	MBR5	Digital Output	**Multibit Modulator Output** – Right channel output bit 5
31	MBR4	Digital Output	**Multibit Modulator Output** – Right channel output bit 4
32	MBR3	Digital Output	**Multibit Modulator Output** – Right channel output bit 3
33	LRCLK	Digital Input/Output	**Left Right Clock** – Indicates whether left or right channel is active on the serial audio data line
34	SCLK	Digital Input/Output	**Serial Clock** – Clock for the serial audio interface

35	RSTB	Digital Input	**Reset** – active low input places devices in a low power mode
38	MBR2	Digital Output	**Multibit Modulator Output** – Right channel output bit 2
39	MBR1	Digital Output	**Multibit Modulator Output** – Right channel output bit 1
40	MBR0	Digital Output	**Multibit Modulator Output** – Right channel output bit 0
41	DCLK	Digital Output	**Clock Out** – Clock for DSD and Multibit outputs
42	DSDR	Digital Output	**DSD Output** – Right channel DSD output
43	DSDL	Digital Output	**DSD Output** – Left channel DSD output
46	SDOUT	Digital Output	**Serial Audio Data Output** – PCM output for left and right channels
47	MBL0	Digital Output	**Multibit Modulator Output** – Left channel output bit 0
48	MBL1	Digital Output	**Multibit Modulator Output** – Left channel output bit 1
49	MBL2	Digital Output	**Multibit Modulator Output** – Left channel output bit 2
50	MBL3	Digital Output	**Multibit Modulator Output** – Left channel output bit 3
51	MBL4	Digital Output	**Multibit Modulator Output** – Left channel output bit 4
52	MBL5	Digital Output	**Multibit Modulator Output** – Left channel output bit 5
53	MDIV	Digital Input	**MCLK Divider** – Enables divide by 2 of master clock
54	HPFB	Digital Input	**Highpass Filter** – Enables digital highpass filter, active low
57	I2S_LJ	Digital Input	**Audio Output Format Select** – Selects either the I^2S or left justified output format, high=I^2S / low=LJ
58	M0	Digital Input	**Mode Selection** – Selects among the following sampling rates: Single, double, quad, and octal
59	M1		
60	OVFLB	Digital Output	**Overflow –** Detects overflow on either channel
61	MCLK	Digital Input	**Master Clock** – Clock for the ΣΔ modulator and digital filters

2. Specifications

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Analog	AVDD	-0.3	+6.0	V
	Digital	DVDD	-0.3	+6.0	V
Analog Input Voltage		V_{INA}	GND-0.7	AVDD+0.7	V
Digital Input Voltage		V_{IND}	GND-0.7	DVDD+0.7	V
Input Current		I_{in}	-10	+10	mA
Ambient Operating Temperature		T_A	-50	+95	ºC
Storage Temperature		T_{stg}	-65	+150	ºC

Recommended Operating Conditions

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Analog	AVDD	4.75	5.0	5.25	V
	Digital	DVDD	3.0	3.3	5.25	V
Ground		GND		0		V
Ambient Operating Temperature		T_A	-10		+70	ºC

Dynamic Electrical Characteristics

Unless otherwise stated, the test conditions are: input signal is a 1kHz sine wave, measurement bandwidth is 20Hz to 20kHz, AVDD=5.0V, DVDD=3.3V, T_A=25 ºC.

Parameters	Symbol	Min	Typ	Max	Units
PCM Output, Single-Speed: F_S=48kHz					
Dynamic Range					
20 kHz, A-weighted	DR	117	123	-	dB
20 kHz, unweighted		115	121	-	dB
THD+N					
20 kHz, -2 dB	THD+N	-100	-105		dB
20 kHz, -20 dB			-100		dB
20 kHz, -60 dB			-60		dB
PCM Output, Double-Speed: F_S=96kHz					
Dynamic Range					
20 kHz, A-weighted	DR	117	123	-	dB
20 kHz, unweighted		115	121	-	dB
40 kHz, unweighted		112	118		dB
THD+N					
20 kHz, -2 dB		-100	-105		dB
20 kHz, -20 dB	THD+N		-100		dB
20 kHz, -60 dB			-60		dB
40 kHz, -2 dB			-105		dB
PCM Output, Quad-Speed: F_S=192kHz					
Dynamic Range					
20 kHz, A-weighted		117	123	-	dB
20 kHz, unweighted	DR	115	121	-	dB
40 kHz, unweighted		112	118		dB
THD+N					
20 kHz, -2 dB			-105		dB
20 kHz, -20 dB	THD+N		-100		dB
20 kHz, -60 dB			-60		dB
40 kHz, -2 dB			-105		dB
PCM Output, Octal-Speed: F_S=384kHz					
Dynamic Range					
20 kHz, A-weighted		117	123	-	dB
20 kHz, unweighted	DR	115	121	-	dB
40 kHz, unweighted		112	118		dB
80 kHz, unweighted		109	115		dB
THD+N					
-2 dB			-105		dB
-20 dB	THD+N		-100		dB
-60 dB			-60		dB
40 kHz bandwidth -2 dB			-105		dB
80 kHz bandwidth -2 dB			-105		dB

Multibit Outputs: F_S=12.288MHz					
Dynamic Range A-weighted Unweighted		 118 116	 124 122	 - -	 dB dB
THD+N -2 dB -20 dB -60 dB	THD+N	-100	 -105 -100 -60		 dB dB dB
DSD Outputs: F_S=12.288MHz					
Dynamic Range A-weighted Unweighted			 112 110	 - -	 dB dB
THD+N -2 dB -20 dB -60 dB	THD+N		 -103 -90 -50		 dB dB dB
Dynamic Performance for All Modes					
Intermodulation distortion (-13dB tones at 18kHz and 19kHz)		-	-128	-	dB
Interchannel Isolation		-	130	-	dB
DC Accuracy					
Channel Level Matching (20kHz input signal)		-	0.1	-	dB
Gain Error		-5	-	5	%
Gain Drift		-	±100	0	ppm/ºC
Offset Error HPF Enabled HPF Disabled		 - -	 0 100	 - -	 LSB LSB
Analog Input Characteristics					
Full Scale Input Voltage (Single Ended)		0.87 x AVDD	0.90 x AVDD	0.93 x AVDD	Vpp
Common Mode Rejection Ratio	CMRR	-	100	-	dB
Input Impedance (Differential)		-	2.0	-	kΩ

Digital Filter Characteristics

Parameters	Symbol	Min	Typ	Max	Units
Filter Response: Single-Speed Mode (2kHz to 54kHz)					
Passband		0		0.42	F_S
Passband Ripple		-0.015		0	dB
Stopband		0.58			F_S
Stopband Attenuation		-100			dB
Total Group Delay (F_S= Output Sample Rate)	t_{gd}		$12/F_S$		s

Filter Response: Double-Speed Mode (50kHz to 108kHz)					
Passband		0		0.44	F_S
Passband Ripple		-0.015		0	dB
Stopband		0.70			F_S
Stopband Attenuation		-117			dB
Total Group Delay (F_S= Output Sample Rate)	t_{gd}		$7/F_S$		s
Filter Response: Quad-Speed Mode (100kHz to 216kHz)					
Passband		0		0.25	F_S
Passband Ripple		-0.015		0	dB
Stopband		0.80			F_S
Stopband Attenuation		-108			dB
Total Group Delay (F_S= Output Sample Rate)	t_{gd}		$5/F_S$		s
Filter Response: Octal-Speed Mode (200kHz to 432kHz)					
Passband (-0.1dB)		0		0.22	F_S
Passband Ripple		-0.015		0	dB
Stopband		0.79			F_S
Stopband Attenuation		-116			dB
Total Group Delay (F_S= Output Sample Rate)	t_{gd}		$5/F_S$		s
High Pass Filter Characteristics					
Single-Speed Mode, F_s=48kHz					
Frequency Response, -3.0dB			0.47		Hz
Passband droop, 20Hz			0.0024		dB
Phase Deviation, 20Hz			1.33		Deg
Filter Settling Time			5.12		s
Double-Speed Mode, F_s=96kHz					
Frequency Response, -3.0dB			0.94		Hz
Passband droop, 20Hz			0.0094		dB
Phase Deviation, 20Hz			2.7		Deg
Filter Settling Time			2.56		s
Quad-Speed Mode, F_s=192kHz					
Frequency Response, -3.0dB			1.9		Hz
Passband droop, 20Hz			0.038		dB
Phase Deviation, 20Hz			5.3		Deg
Filter Settling Time			1.28		s
Octal-Speed Mode, F_s=384kHz					
Frequency Response, -3.0dB			3.7		Hz
Passband droop, 20Hz			0.15		dB
Phase Deviation, 20Hz			10.6		Deg
Filter Settling Time			0.64		s

Digital Filter Frequency Response Plots

Single-Speed Mode

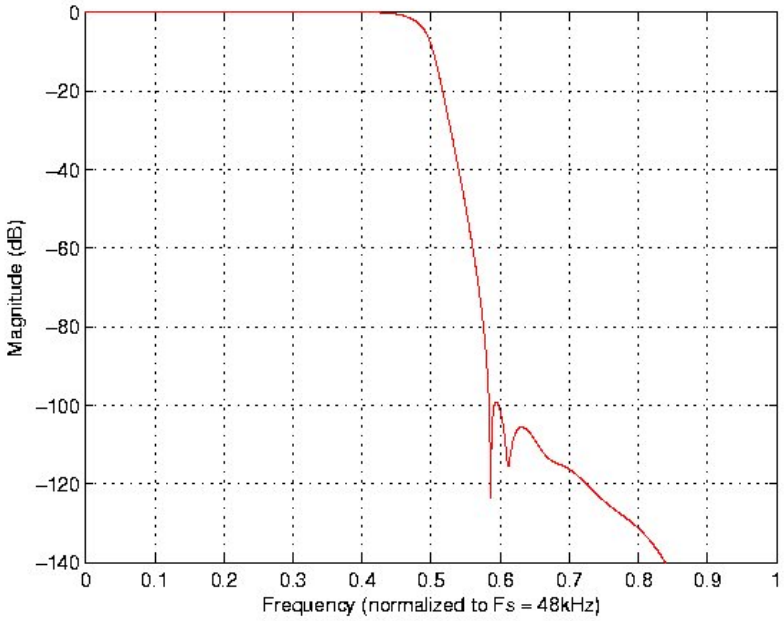


Figure 1: Frequency response, single-speed filter

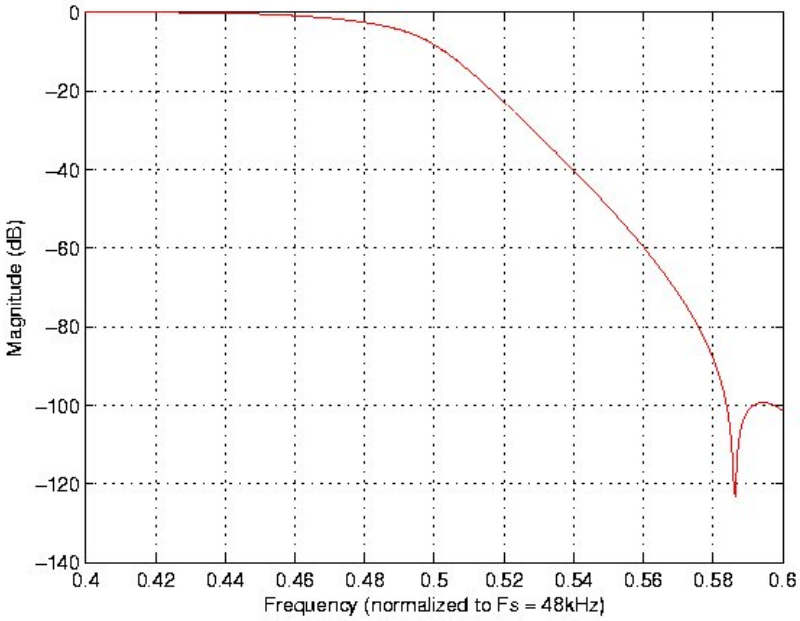


Figure 2: Transition band response, single-speed filter

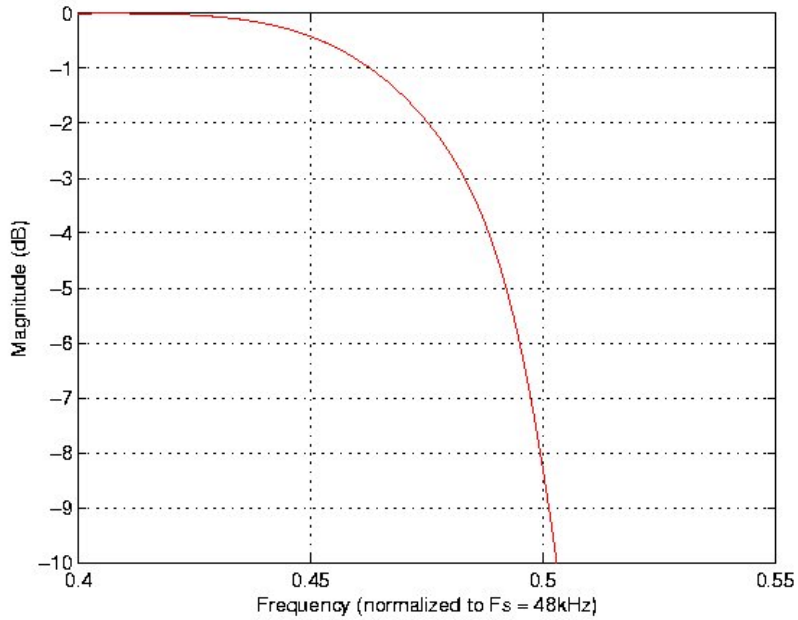


Figure 3: Band edge response, single-speed filter

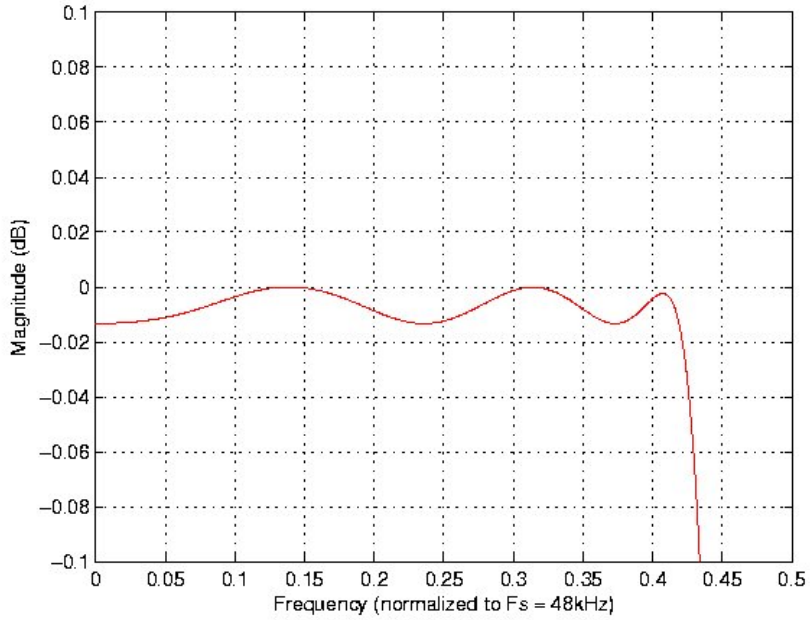


Figure 4: Passband response, single-speed filter

Double-Speed Mode

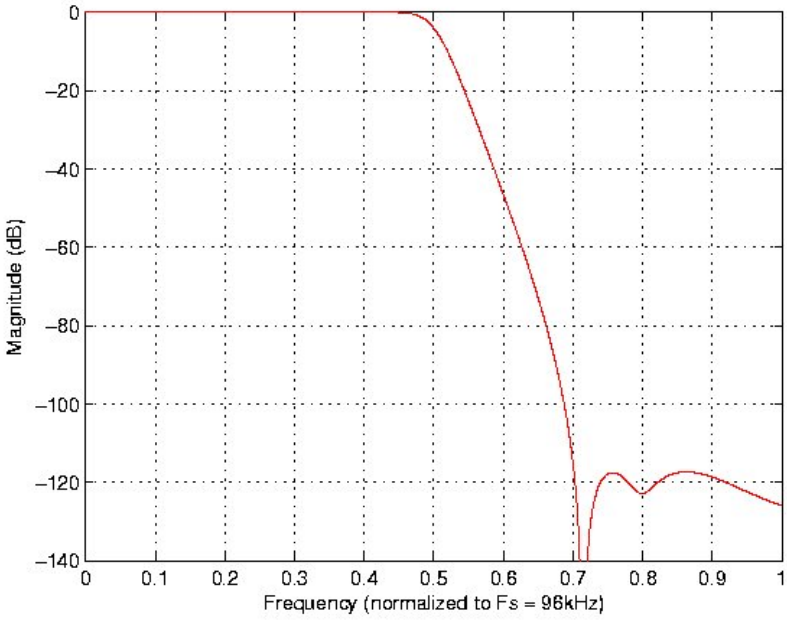


Figure 5: Frequency response, double-speed filter

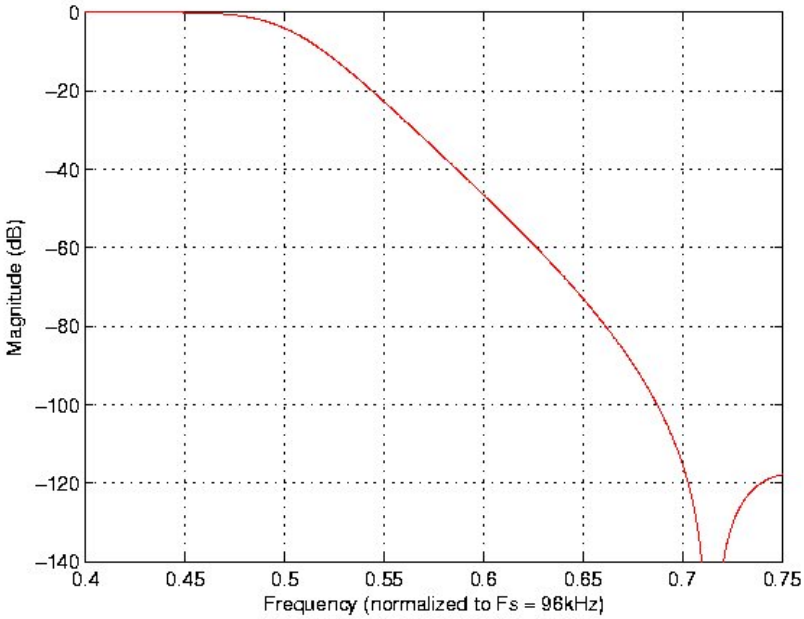


Figure 6: Transition band response, double-speed filter

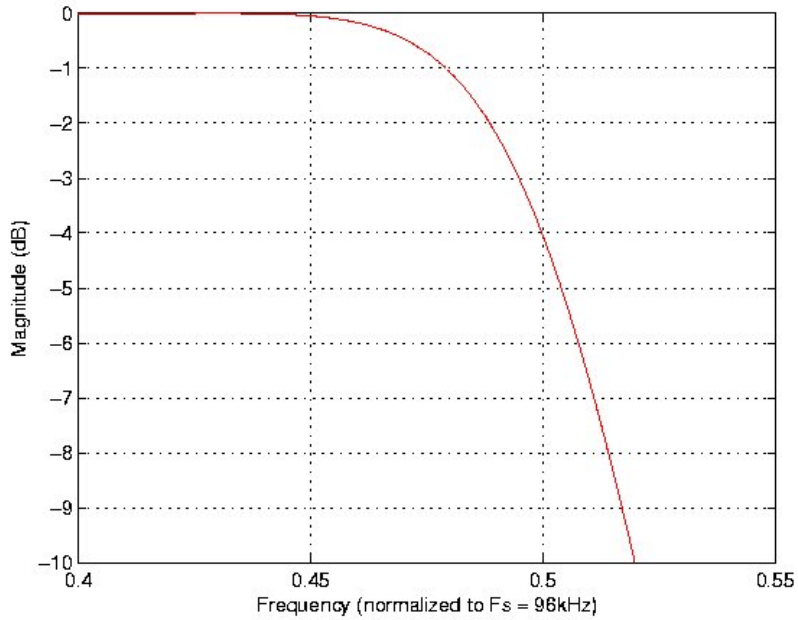


Figure 7: Band edge response, double-speed filter

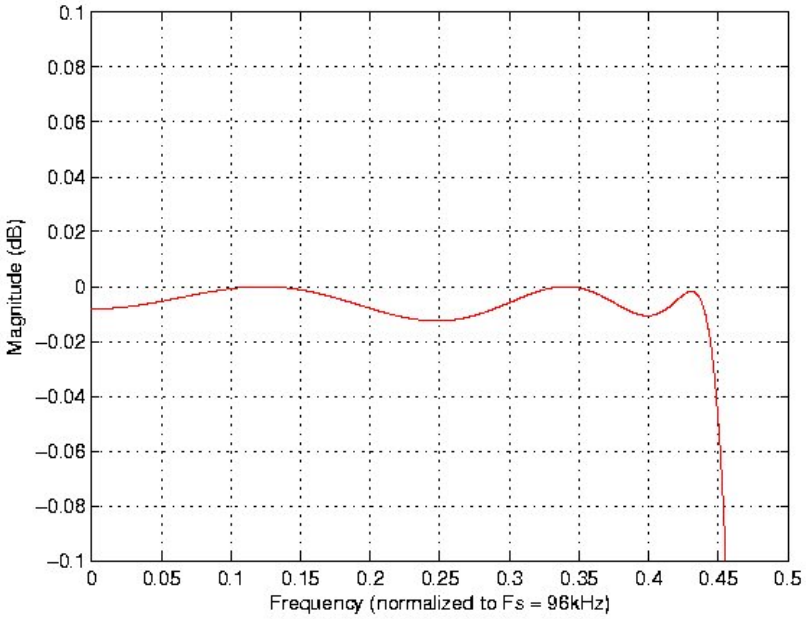


Figure 8: Passband response, double-speed filter

Quad-Speed Mode

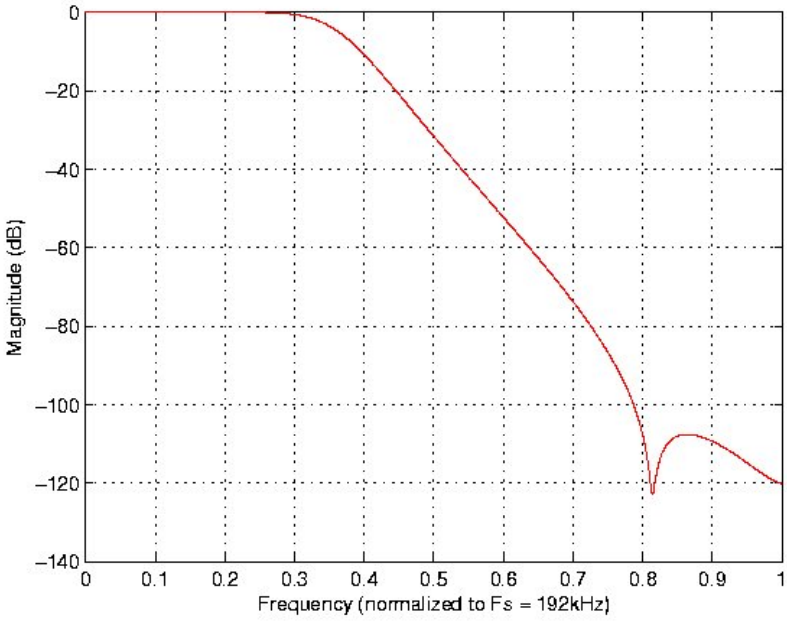


Figure 9: Frequency response, quad-speed filter

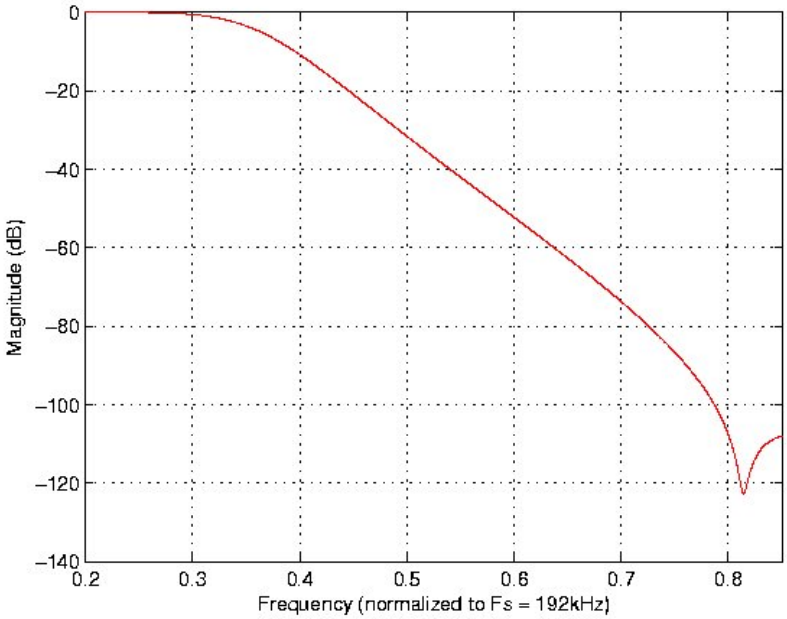


Figure 10: Transition band response, quad-speed filter

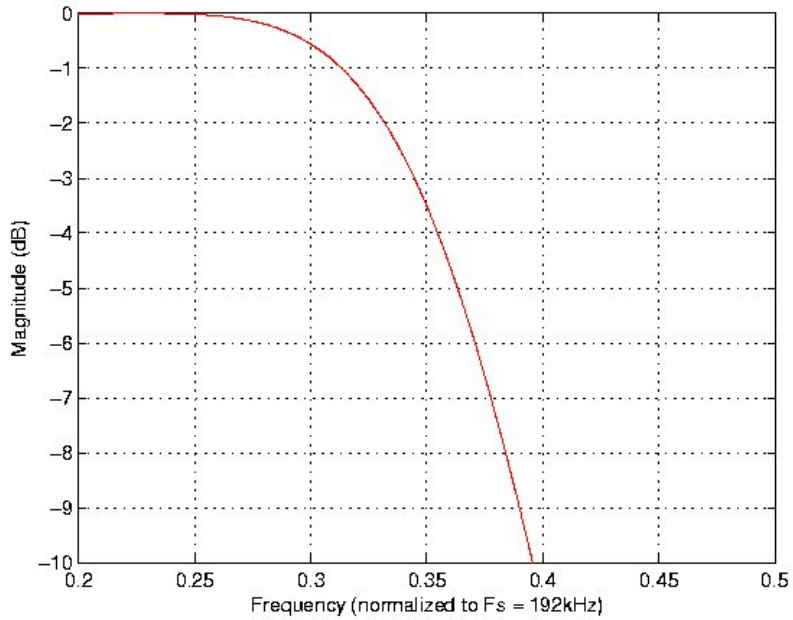


Figure 11: Band edge response, quad-speed filter

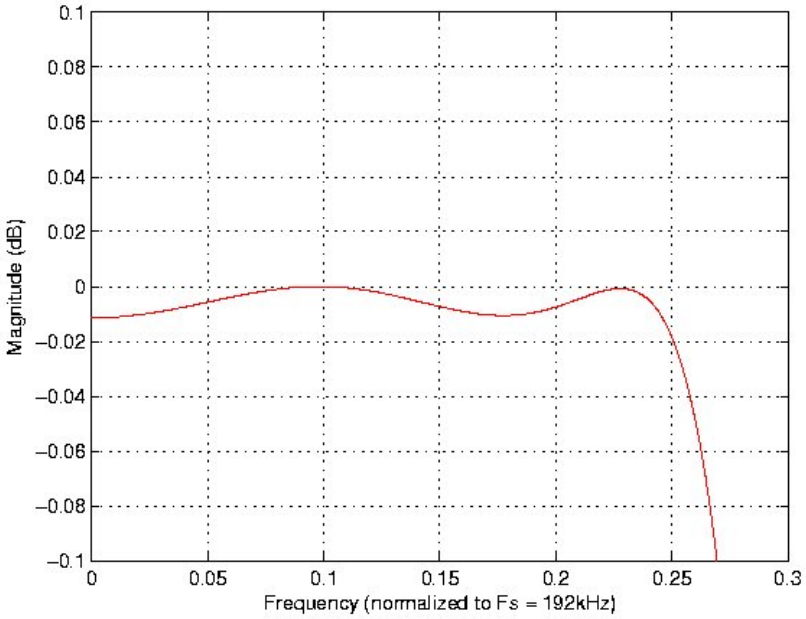


Figure 12: Passband response, quad-speed filter

Octal-Speed Mode

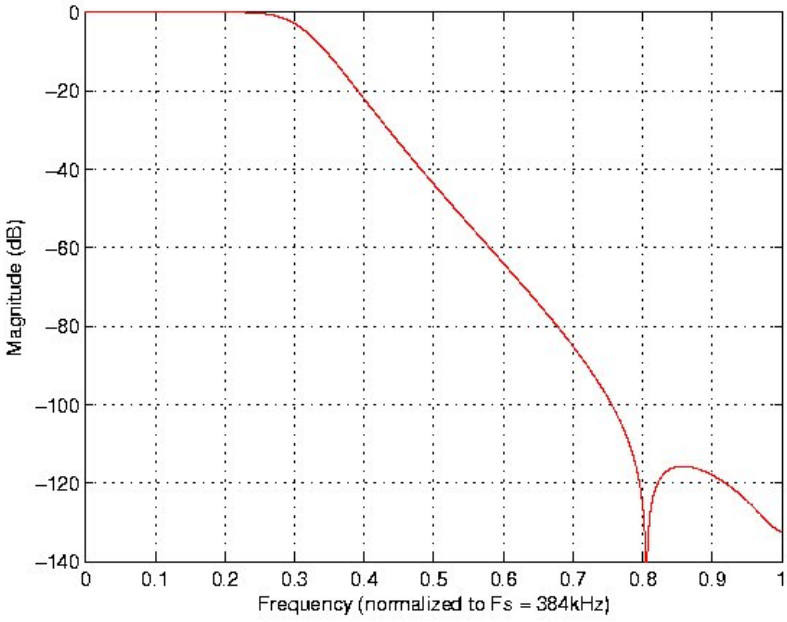


Figure 13: Frequency response, octal-speed filter

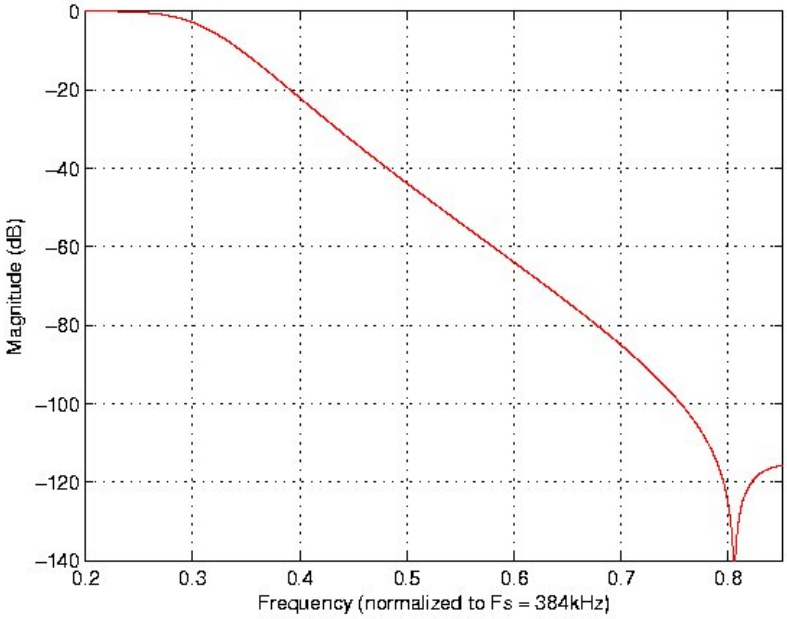


Figure 14: Transition band response, octal-speed filter

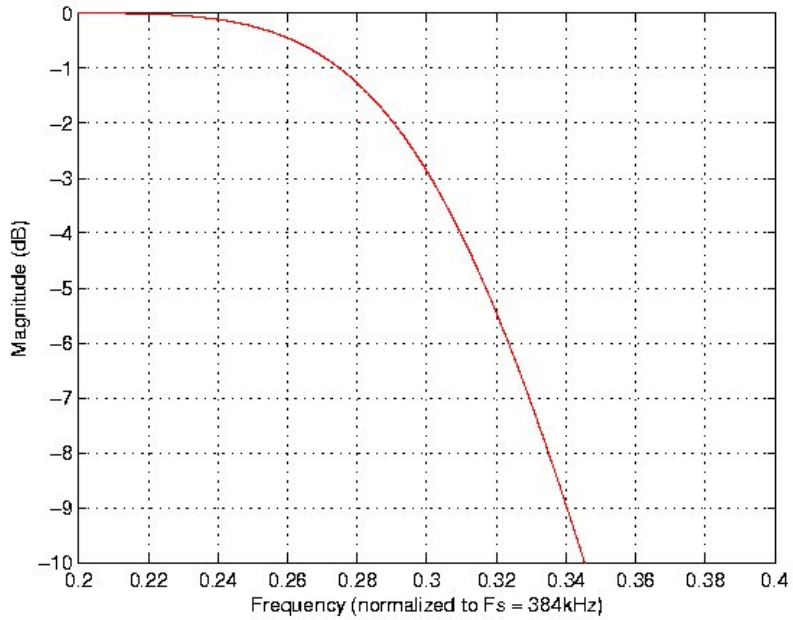


Figure 15: Transition band response, octal-speed filter

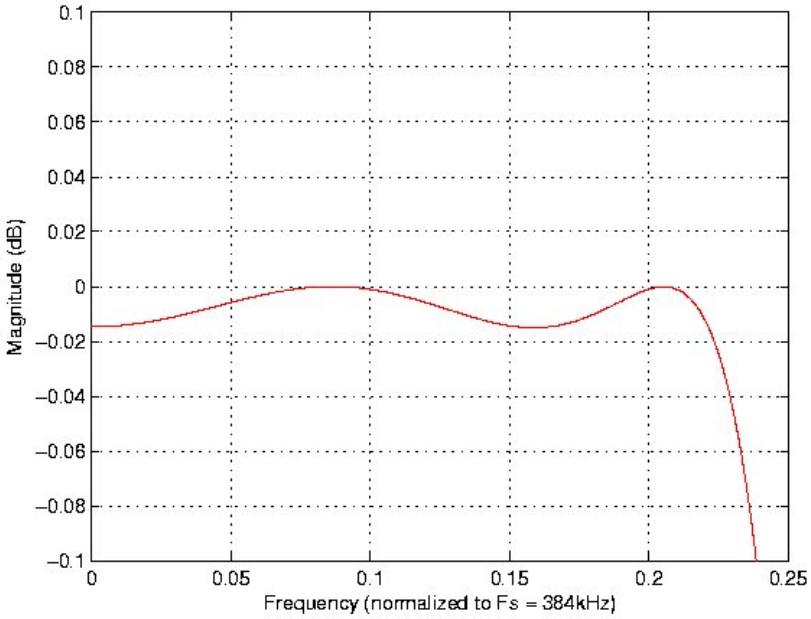


Figure 16: Passband response, octal-speed filter

Digital Filter Impulse Response Plots

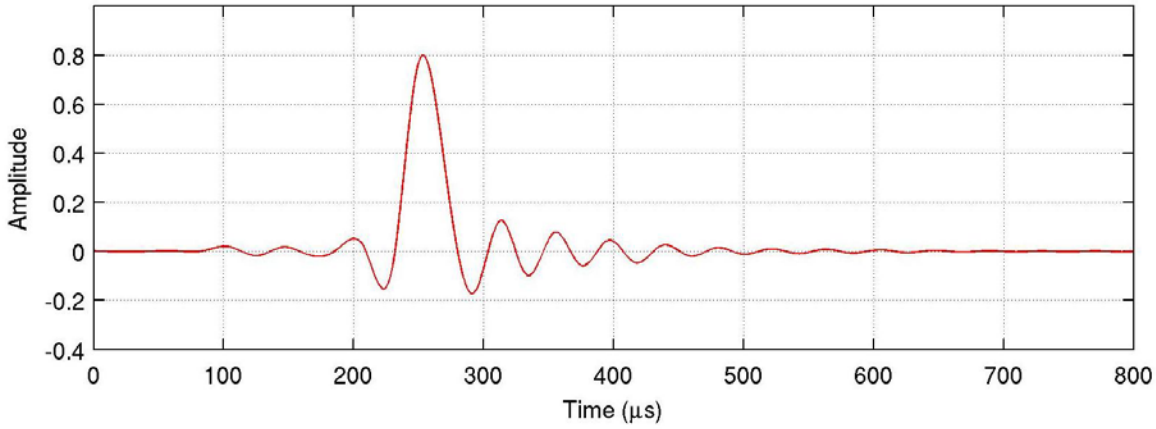


Figure 17: Single-speed filter

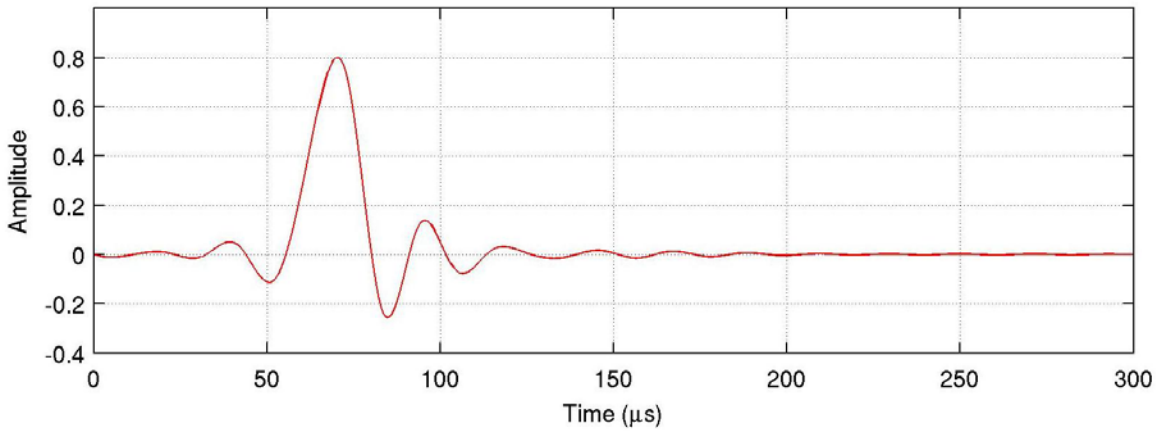


Figure 18: Double-speed filter

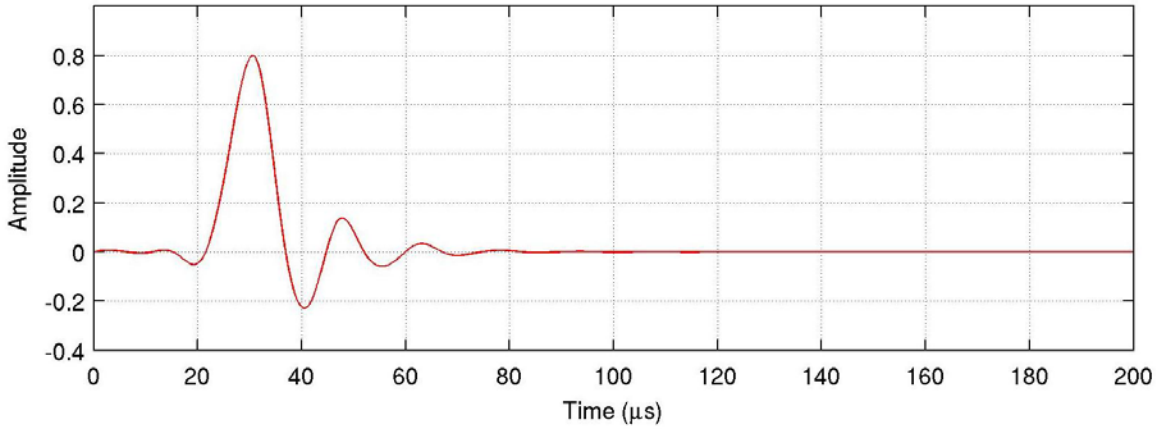


Figure 19: Quad-speed filter

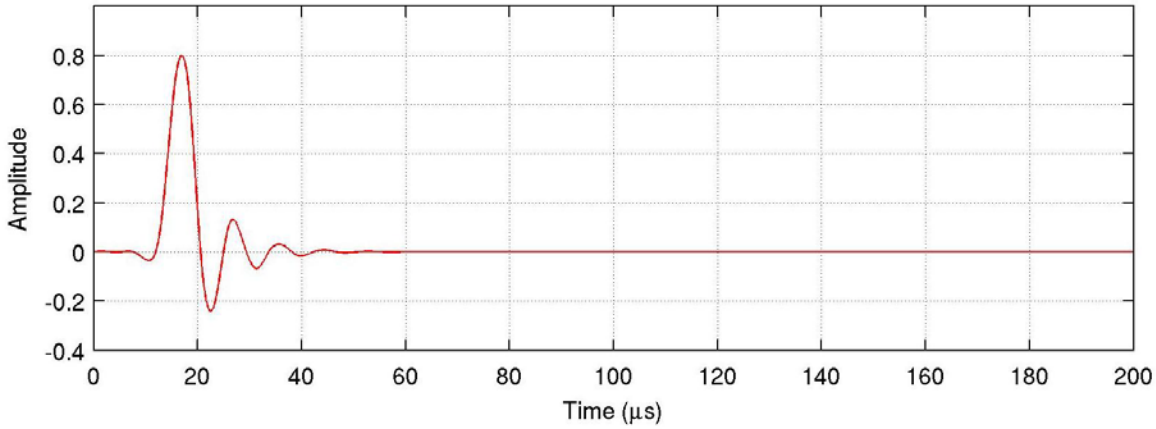


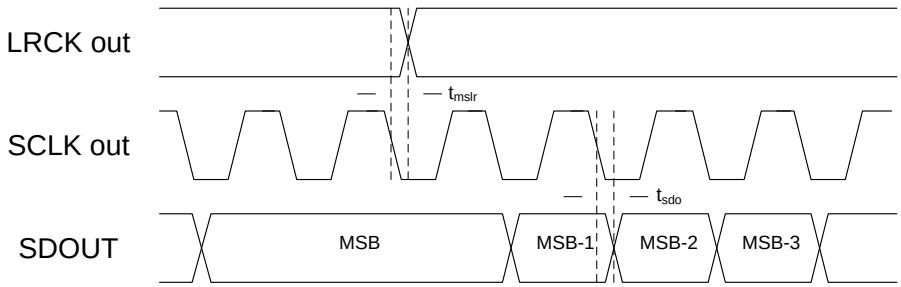
Figure 20: Octal-speed filter

Switching Characteristics

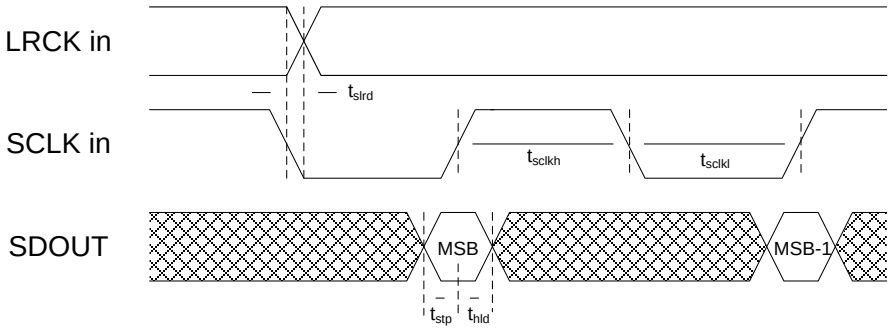
Conditions: Logic "0" = 0V, Logic "1" = DVDD, C_L = 20pF, DVDD = 3.3V

Parameter		Symbol	Min	Typ	Max	Unit
Output Sample Rate	Single-Speed Mode	F_S	2	-	54	kHz
	Double-Speed Mode	F_S	50	-	108	kHz
	Quad-Speed Mode	F_S	100	-	216	kHz
	Octal-Speed Mode	F_S	200	-	432	kHz
OVFL to LRCK Edge Setup Time		t_{setup}	$16/f_{sclk}$	-	-	s
OVFL to LRCK Edge Hold Time		t_{hold}	$1/f_{sclk}$	-	-	s
OVFL time-out			-	680	-	ms
MCLK Specifications						
MCLK Period			36.2	-	1953	ns
MCLK Frequency, MDIV=0			-	12.288	13.824	MHz
MCLK Frequency, MDIV=1			-	24.576	27.648	MHz
MCLK Duty Cycle			45	-	55	%
Master Mode						
SCLK falling to LRCK transition		t_{mslr}	-4	0	4	ns
SCLK falling to SDOUT valid		t_{sdo}	-	-	5	ns
SCLK Duty Cycle			-	50	-	%
Slave Mode						
Single Speed						
Output Sample Rate		F_S	2	-	54	kHz
LRCK Duty Cycle			40	50	60	%
SCLK Period		t_{sclk}	290	-	-	ns
SCLK Duty Cycle			45	50	55	%
SDOUT valid before SCLK rising		t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising		t_{hld}	5	-	-	ns
SCLK falling to LRCK transition		t_{slrd}	-20	-	20	ns
Double Speed						
Output Sample Rate		F_S	50	-	108	kHz
LRCK Duty Cycle			40	50	60	%
SCLK Period		t_{sclk}	145	-	-	ns
SCLK Duty Cycle			45	50	55	%
SDOUT valid before SCLK rising		t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising		t_{hld}	5	-	-	ns
SCLK falling to LRCK transition		t_{slrd}	-20	-	20	ns
Quad Speed						
Output Sample Rate		F_S	100	-	216	kHz
LRCK Duty Cycle			40	50	60	%
SCLK Period		t_{sclk}	72	-	-	ns
SCLK Duty Cycle			45	50	55	%
SDOUT valid before SCLK rising		t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising		t_{hld}	5	-	-	ns
SCLK falling to LRCK transition		t_{slrd}	-8	-	8	ns

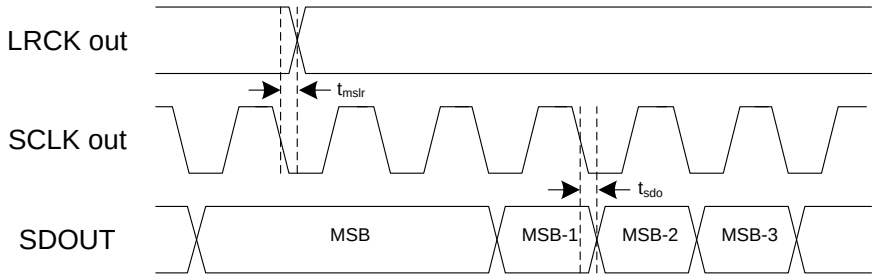
Octal Speed					
Output Sample Rate	F_S	200	-	432	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclk}	36	-	-	ns
SCLK Duty Cycle		45	50	55	%
SDOUT valid before SCLK rising	t_{stp}	5	-	-	ns
SDOUT valid after SCLK rising	t_{hld}	5	-	-	ns
SCLK falling to LRCK transition	t_{slrd}	-8	-	8	ns
DSDR/DSDL and MBR/MBL					
DCLK period, MDIV=0	t_{DCLK}		$1/f_{sclk}$		s
DCLK period, MDIV=1	t_{DCLK}		$1/2f_{sclk}$		s
DSDx/MBx valid to DCLK rising	t_{MBDC}	10			ns
DCLK rising to DSDx/MBx not valid	t_{DCMB}			10	ns



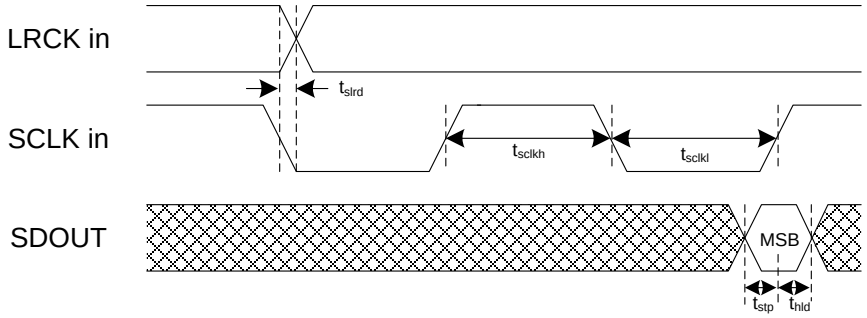
Master Mode, Left-Justified



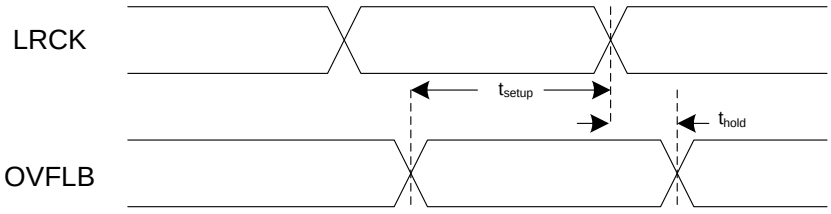
Slave Mode, Left-Justified



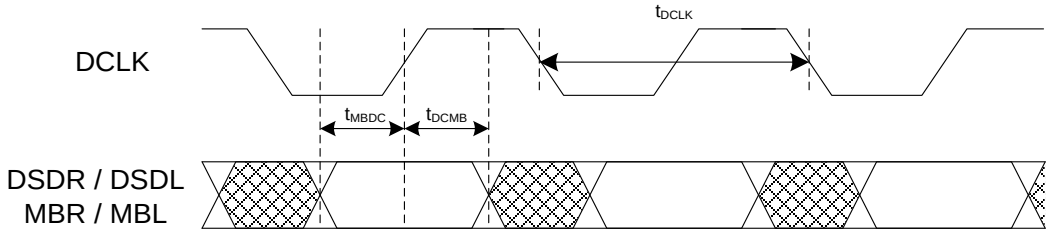
Master Mode, I^2S



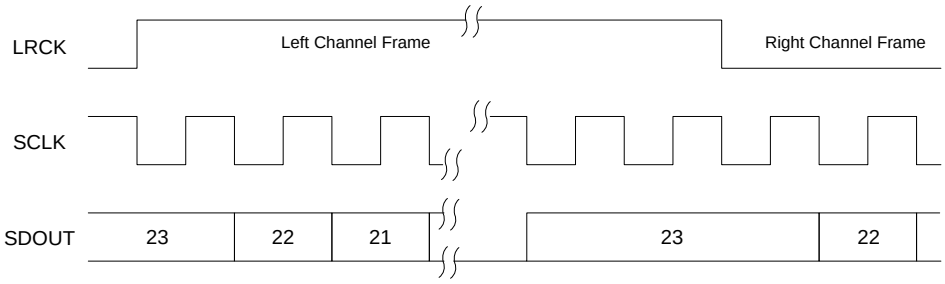
Slave Mode, I^2S



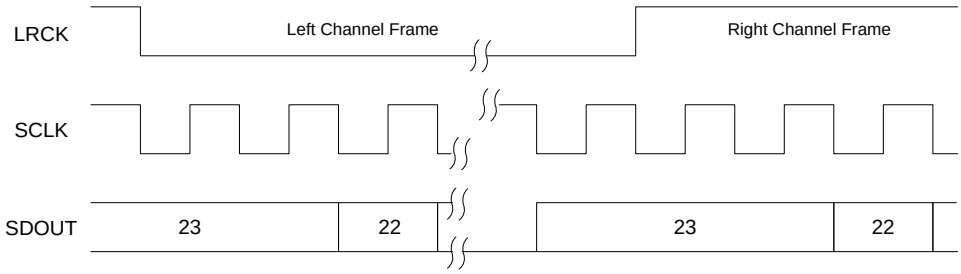
OVFLB Timing



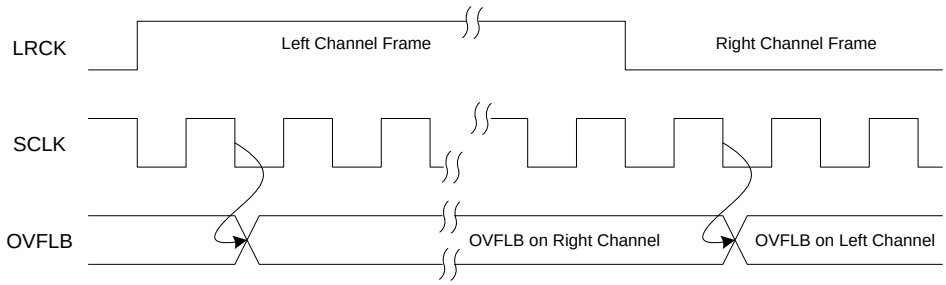
DSD and MB timing



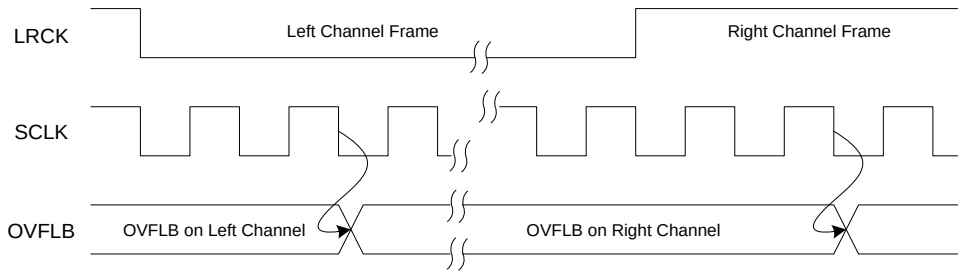
SDOUT Timing, Left-Justified



SDOUT Timing, I^2S



OVFLB Timing, Left-Justified



OVFLB Timing, I^2S

DC Electrical Characteristics

All parameters are specified at T_A = +25ºC, GND = 0V, all voltages with respect to ground. MCLK = 24.576 MHz; Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current					
AVDD = 5V	I_A	-	128	-	mA
PCM Single Speed Mode					
DVDD = 5V	I_D	-	26	-	mA
DVDD = 3.3V	I_D	-	17	-	mA
PCM Double Speed Mode					
DVDD = 5V	I_D	-	32	-	mA
DVDD = 3.3V	I_D	-	21	-	mA
PCM Quad Speed Mode					
DVDD = 5V	I_D	-	38	-	mA
DVDD = 3.3V	I_D	-	25	-	mA
PCM Octal Speed Mode					
DVDD = 5V	I_D	-	56	-	mA
DVDD = 3.3V	I_D	-	37	-	mA
DSD Mode					
DVDD = 5V	I_D	-	2	-	mA
DVDD = 3.3V	I_D	-	1	-	mA
Multibit Mode					
DVDD = 5V	I_D	-	6	-	mA
DVDD = 3.3V	I_D	-	4	-	mA
Power Supply Current AVDD = 5V (Power-Down Mode[8]) DVDD = 5V	I_A	-	250	-	µA
	I_D	-	50	-	µA
Power Consumption					
PCM Single Speed Mode					
AVDD = DVDD = 5V	P_t	-	770	-	mW
AVDD = 5V, DVDD = 3.3V	P_t	-	696	-	mW
PCM Double Speed Mode					
AVDD = DVDD = 5V	P_t	-	800	-	mW
AVDD = 5V, DVDD = 3.3V	P_t	-	709	-	mW
PCM Quad Speed Mode					
AVDD = DVDD = 5V	P_t	-	830	-	mW
AVDD = 5V, DVDD = 3.3V	P_t	-	723	-	mW
PCM Octal Speed Mode					
AVDD = DVDD = 5V	P_t	-	920	-	mW
AVDD = 5V, DVDD = 3.3V	P_t	-	762	-	mW
DSD Mode					
AVDD = DVDD = 5V	P_t	-	650	-	mW
AVDD = 5V, DVDD = 3.3V	P_t	-	643	-	mW
Multibit Mode					
AVDD = DVDD = 5V	P_t	-	670	-	mW
AVDD = 5V, DVDD = 3.3V	P_t	-	653	-	mW
Power-Down Mode	P_t	-	1.5	-	mW
Power Supply Rejection Ratio (1kHz, 25mVpp applied to AVDD, DVDD)	PSRR	-	70	-	dB

CMREF Nominal Voltage		-	2.5	-	V
Output Impedance		-	2.2	-	kΩ
Maximum allowable DC current source/sink		-	0.01	-	mA
REFPR / REFPL Nominal Voltage		-	4.8	-	V
Output Impedance		-	130	-	Ω
Maximum allowable DC current source/sink		-	0.1	-	mA
BUFREF Nominal Voltage		-	2.4	-	V
Output Impedance		-	14.5	-	kΩ
Maximum allowable DC current source/sink		-	0.01	-	mA

[8] Power down mode entered when $\overline{RST}$ = Low and all clocks and data lines are held static.

Digital Characteristics

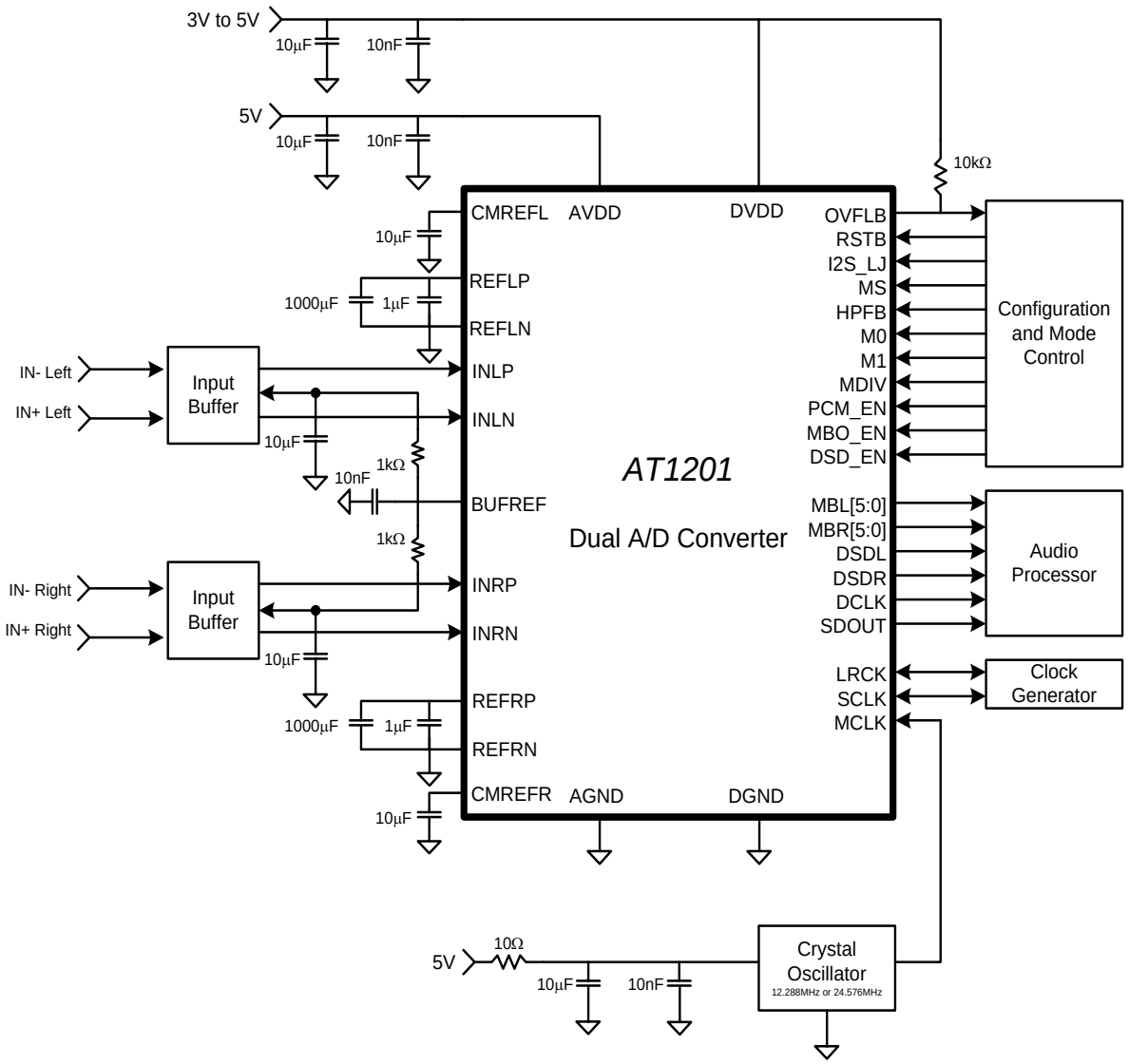
Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage (% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage (% of VL)	V_{IL}	-	-	30%	V
High-Level Output Voltage at I_O = 100 µA (% of VL)	V_{OH}	70%	-	-	V
Low-Level Output Voltage at I_O = 100 µA (% of VL)	V_{OL}	-	-	15%	V
Input Leakage Current	I_{IN}	-10	-	10	µA
OVFLB Current Sink	I_{OVFL}	4	-	-	mA

Thermal Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Maximum Junction Temperature	T_{jmax}	-	-	135	°C
Junction to Ambient Thermal Resistance	$\theta_{JA\text{-}QFN}$	-	31	-	°C/W

Typical Connection to the AT1201

For more detailed information about schematic considerations, consult application note *AN-AT1201-1: Design and Layout Guidelines.*



3. Applications

DSD Output

The AT1201 enters DSD output mode when the DSD_EN pin is pulled high. Bit streams running at MCLK or MCLK/2, depending on the state of MDIV, are generated at the DSDL/DSDR pins. Furthermore, a full rate clock signal, DCLK, is provided to facilitate the acquisition of the DSD data. The DSD output rate is 256x.

Multibit Output

The AT1201 enters multibit output mode when the MBO_EN pin is pulled high. Bit streams running at MCLK or MCLK/2, depending on the state of MDIV, are generated at the MBL[5:0]/MBR[5:0] pins. Furthermore, a full rate clock signal, DCLK, is provided to facilitate the acquisition of the multibit data. The multibit data is represented in two's complement form. The multibit modulator output rate is 256x.

	MDIV = 0	**MDIV = 1**
MCLK/DCLK	1	2

PCM Mode Sampling Range Selection

The mode selection pins, M0 and M1, together with the clock divider pin, MDIV, can be used to select the output sample rate, F_S.

MCLK	**MDIV**	**M1**	**M0**	**Mode**	**Output Sample Rate (F_S)**
256x	0	0	0	Single-Speed Mode	2kHz – 54kHz
256x	0	0	1	Double-Speed Mode	50kHz – 108kHz
256x	0	1	0	Quad-Speed Mode	100kHz – 216kHz
512x	1	0	0	Single-Speed Mode	2kHz – 54kHz
512x	1	0	1	Double-Speed Mode	50kHz – 108kHz
512x	1	1	0	Quad-Speed Mode	100kHz – 216kHz
512x	0	1	1	Octal-Speed Mode	200kHz – 432kHz

Combinations of MDIV, M1, M0, and MCLK rate other than those shown above are invalid. Note that the only way to operate at octal speed mode is for the MCLK frequency to be 512x, or nominally 24.576MHz.

PCM Output Format Selection

The AT1201 can produce both I^2S and LJ (left justified) formatted PCM output. The format selection is made by setting the package pin, I2S_LJ as shown in the Table below.

	I2S_LJ = 0	**I2S_LJ = 1**
PCM Format	LJ	I^2S

Master Clock

The master clock signal, MCLK, is the only logic signal that operates at the AVDD voltage. All other logic signals run at the DVDD level. The clocking interface circuitry within the AT1201 has been engineered to achieve the best possible performance with a 5V master clock.

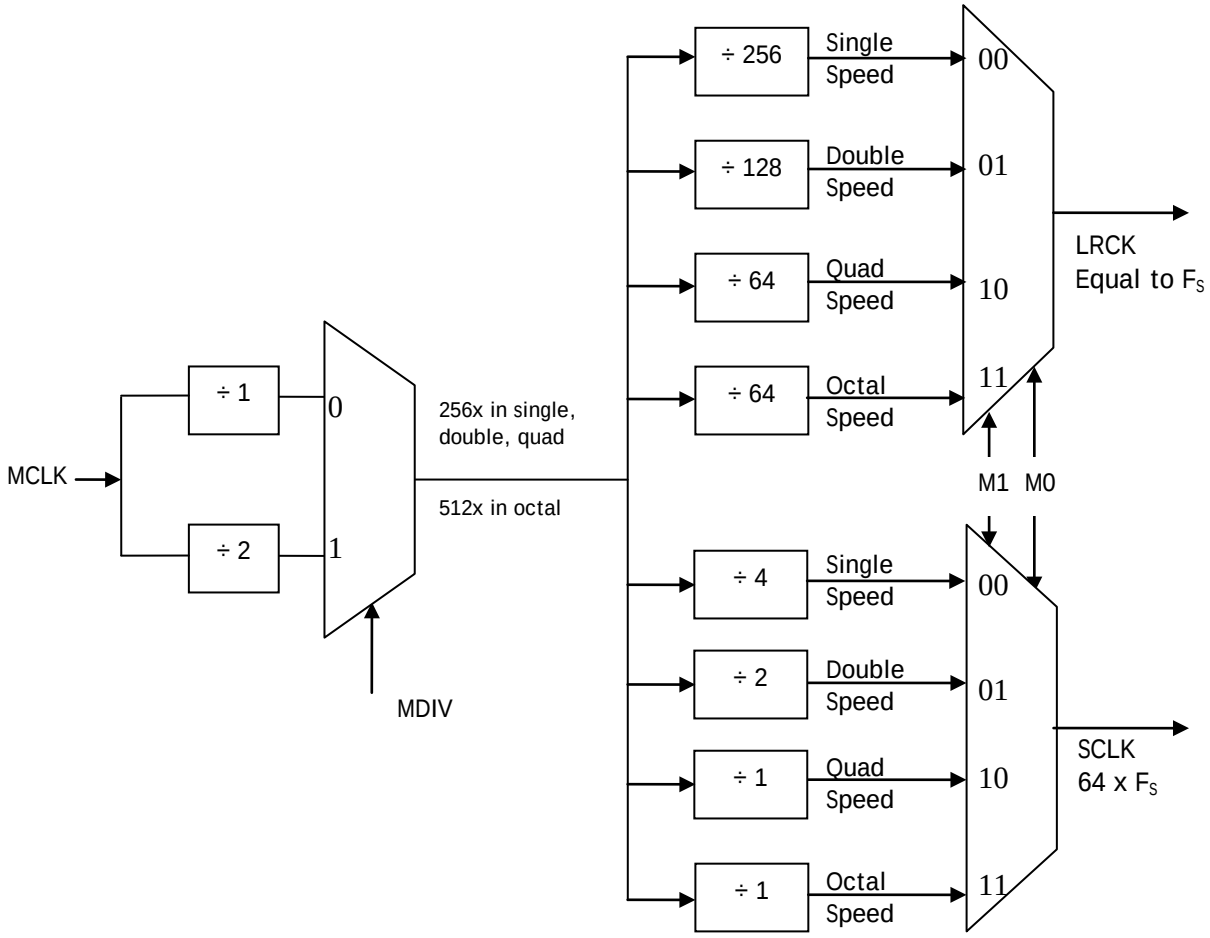
System Clocking

The pin, MS, selects operation in PCM master or slave mode. In Master Mode, LRCK and SCLK are generated synchronously on-chip. In Slave Mode, LRCK and SCLK are generated externally and are inputs to the device. In addition, in Master Mode the MDIV input is used to internally divide the master clock.

	MS = 0	MS = 1
Clock Mode	Slave	Master

Master Mode

In Master Mode the internally generated LRCK and SCLK clocks function as outputs. The LRCK is equal to F_S, the sampling frequency, and the SCLK is equal to 64xF_S. Note that to operate in octal speed mode, MCLK must be a 512x clock, MDIV must be set low, and M1/M0 must both be set high.



Slave Mode

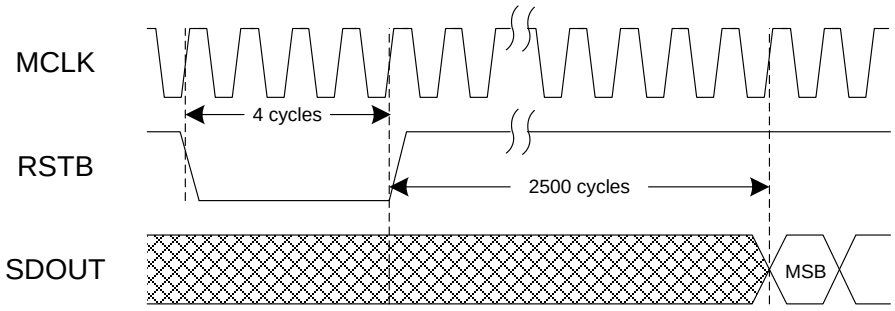
In Slave mode the SCLK and LRCK are inputs. It is recommended that both the LRCK and SCLK be generated synchronously with the MCLK. In addition, it is recommended that LRCK be equal to F_S, the sampling frequency, and the SCLK should be equal to 64 x F_S.

	Single-Speed F_S=2kHz-54kHz	**Double-Speed F_S=50kHz-108kHz**	**Quad-Speed F_S=100kHz-216kHz**	**Octal-Speed F_S=200kHz-432kHz**
MCLK/LRCK	256x, 512x	128x, 256x	64x, 128x	64x
SCLK/LRCK	64x	64x	64x	64x

Power-Up Sequence

The AT1201 has an active low reset pin, RSTB. The device should be maintained in reset till power supplies, clocks and configuration pins are stable or be placed in reset if any of the supply voltages drop below their minimum operating voltages. RSTB must be asserted for at least 4 cycles of MCLK.

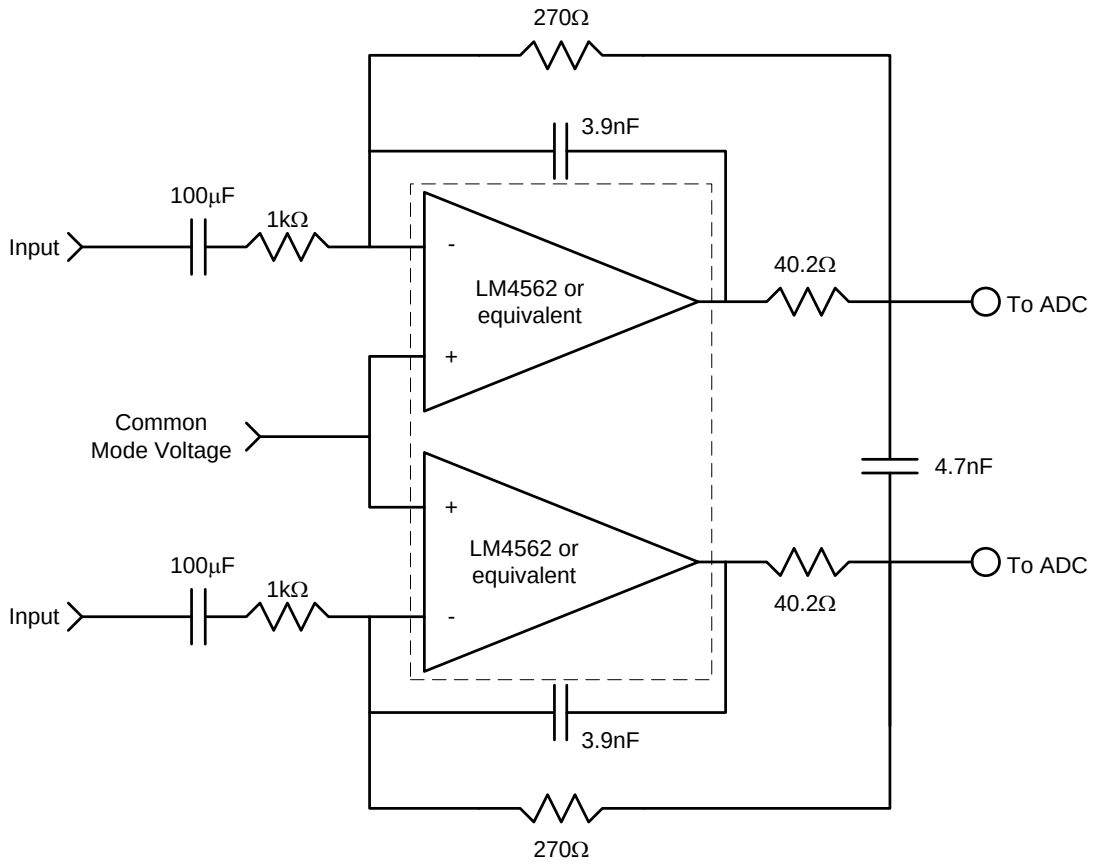
For the device to produce valid data, all internal reference voltages should be stable. To ensure the output data is valid, there is an internal delay, less than 2500 LRCK cycles, between the reset pin going high and the generation of valid outputs. When RSTB is asserted, SDOUT holds its last state.



Reset to Data Valid Timing

Input Buffer Design

It is critical to design a high performance input buffer to achieve optimum performance with the AT1201. The input buffer must be able to drive the switched-capacitor input impedance of the modulator as well as provide anti-aliasing at multiples of the sampling rate, which is nominally 12.288MHz. The circuits shown below achieve both of these goals. Note that feedback capacitor around the operational amplifier should be a C0G type with low voltage coefficient. The inverting buffer configuration is recommended. For more detailed information regarding the input buffer schematic, consult application note *AN-AT1201-1: Design and Layout Guidelines*.



Simplified Input Buffer Circuit (see AN-AT1201-1 for more details)

Highpass Filter and DC Offset Calibration

The AT1201 has a digital highpass filter that can be used to remove DC offset. By disabling the highpass filter after the filter has settled, the offset is frozen and continues to be subtracted from the output result. Therefore, the filter can either continuously track the offset, or it can capture the offset during a calibration cycle, then be disabled.

Overflow Detection

The AT1201 detects overflow on each input channel. The active low OVFLB signal is time multiplexed with LRCK for ease of latching. After an overflow condition has been detected, OVFLB remains asserted as indicated on page 8. Each channel can enter the overflow condition independently of the other. If both channels are in overflow at the same time, they exit overflow simultaneously, after the timeout period has expired on the last channel to enter overflow.

The OVFLB signal is asserted one SCLK period after an LRCK transition in left-justified mode. In this mode, the rising edge of LRCK latches the right channel overflow condition, while the falling edge of LRCK latches that of the left channel.

The OVFLB signal is asserted two SCLK periods after an LRCK transition in I^2S mode. In this mode, the rising edge of LRCK latches the left channel overflow condition, while the falling edge of LRCK latches that of the right channel.

The OVFLB signal is an open-drain signal requiring a 10kΩ pull up resistor to DVDD on the PC board. This allows multiple AT1201 devices to share a single pull up resistor to form a wired-OR function.

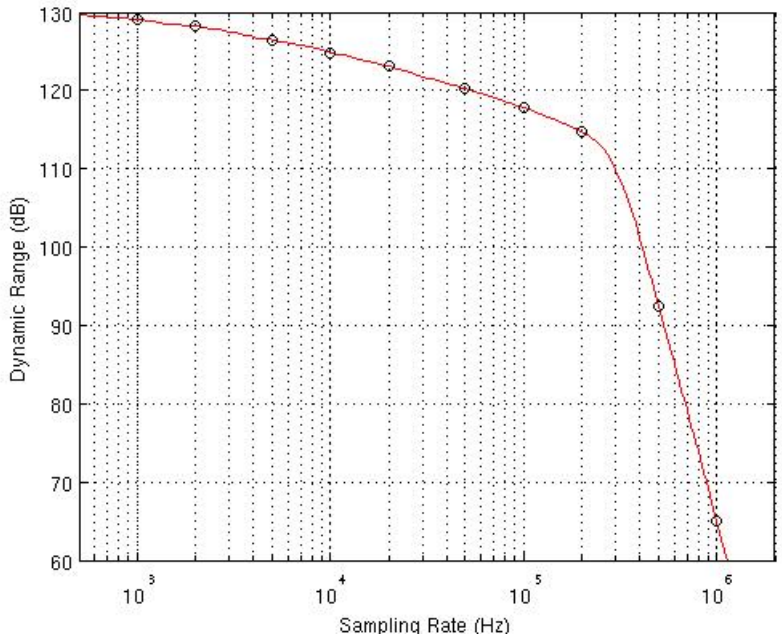
Synchronization of Multiple Devices

When multiple ADCs are required within a system, attention should be paid to ensure simultaneous sampling. When only a single MCLK is needed, then one AT1201 can be placed in master mode and the rest of the AT1201s are in slave mode to the master. If multiple MCLKs are required, then, one possible solution is to have all the clocks generated from the same external source and timing the reset of all the AT1201s to the falling edge of the MCLK, thus ensuring all converters begin sampling on the same clock edge.

Broadband Spectrum

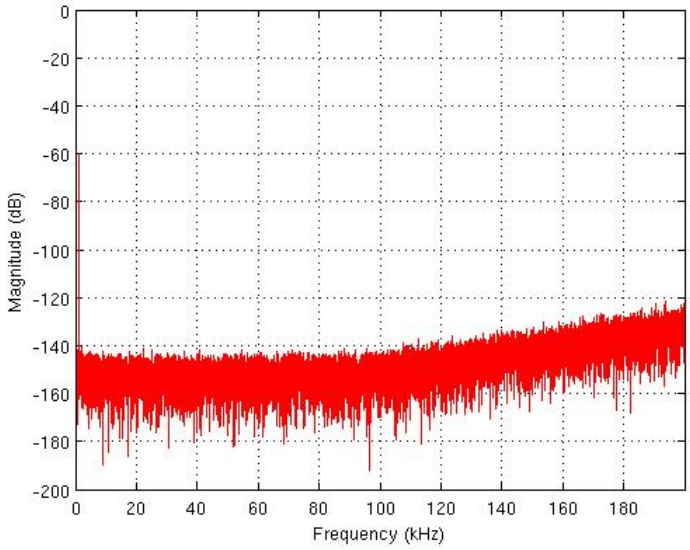
The AT1201 has extremely low and well behaved quantization noise far past the audio band. The spectrum is white to 100kHz, then rises gently. Therefore, operating at quad and octal rates does not introduce any high frequency spikes in the output spectrum that could adversely affect audio processing equipment.

The plot below shows the measured unweighted, dynamic range of the multibit outputs versus sampling frequency when using a sharp decimation filter. At Fs=200kHz, the dynamic range is 114.8dB and at Fs=400kHz it is 103dB. At Fs=1kHz, the dynamic range is 129dB.



Measured Unweighted Dynamic Range vs. Sampling Frequency

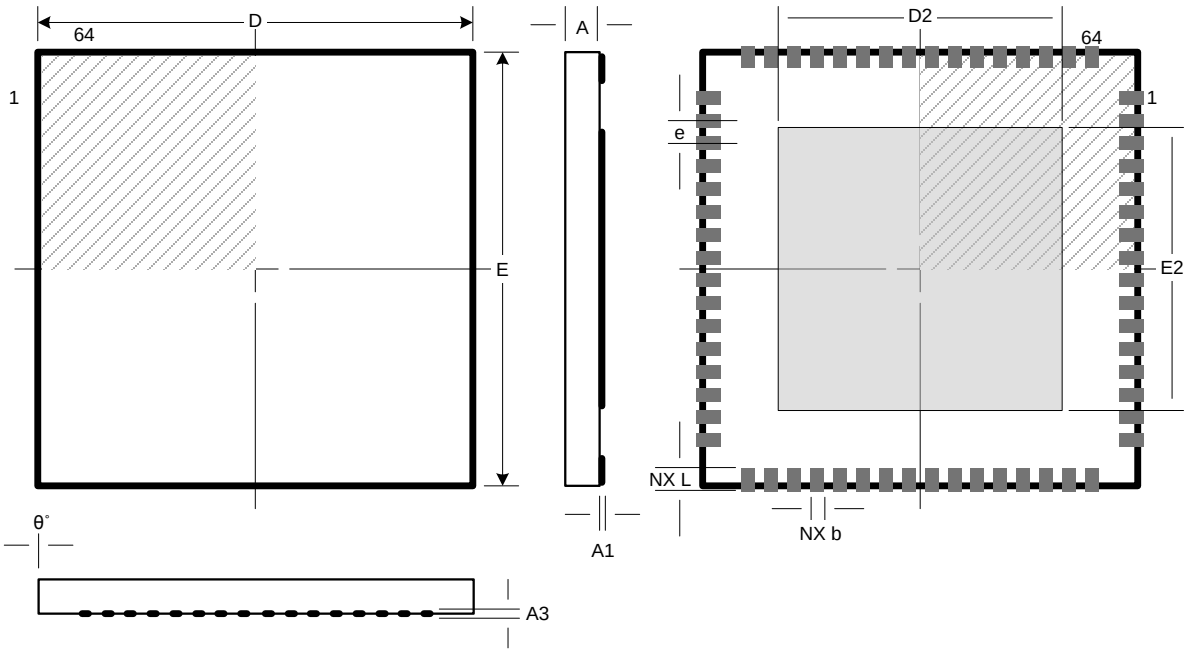
The output spectrum, illustrated below, shows a white and flat character up to 100kHz. Above 100kHz, it continues to be well behaved and rises gently. This plot demonstrates the suitability of the AT1201 for high-speed audio conversion at Fs=192kHz and Fs=384kHz.



Measured Spectrum of Multi-bit Outputs to 200kHz

4. Package Dimensions

64-QFN Package Drawing



JEDEC #	MO 220 / WMMD			
Type	64 Lead			
Dimension	mm		mils	
Symbol	Min	Max	Min	Max
A	0.70	0.80	27.56	31.49
A1	0	0.05	0	1.97
A3	0.175	0.225	6.89	8.86
D	8.9	9.1	350.39	358.27
E	8.9	9.1	350.39	358.27
D2	6.13	6.23	241.34	245.28
E2	6.13	6.23	241.34	245.28
e	0.5 BSC		19.69 BSC	
NX b	0.20	0.30	7.87	11.81
NX L	0.35	0.45	13.78	17.71
θ°	0°	4°	0°	4°

The package features an exposed pad denoted by dimensions D2 and E2. The pad should be soldered to the board's analog ground plane. See the application note *AN-AT1201-1 Design and Layout Guidelines* for details.

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